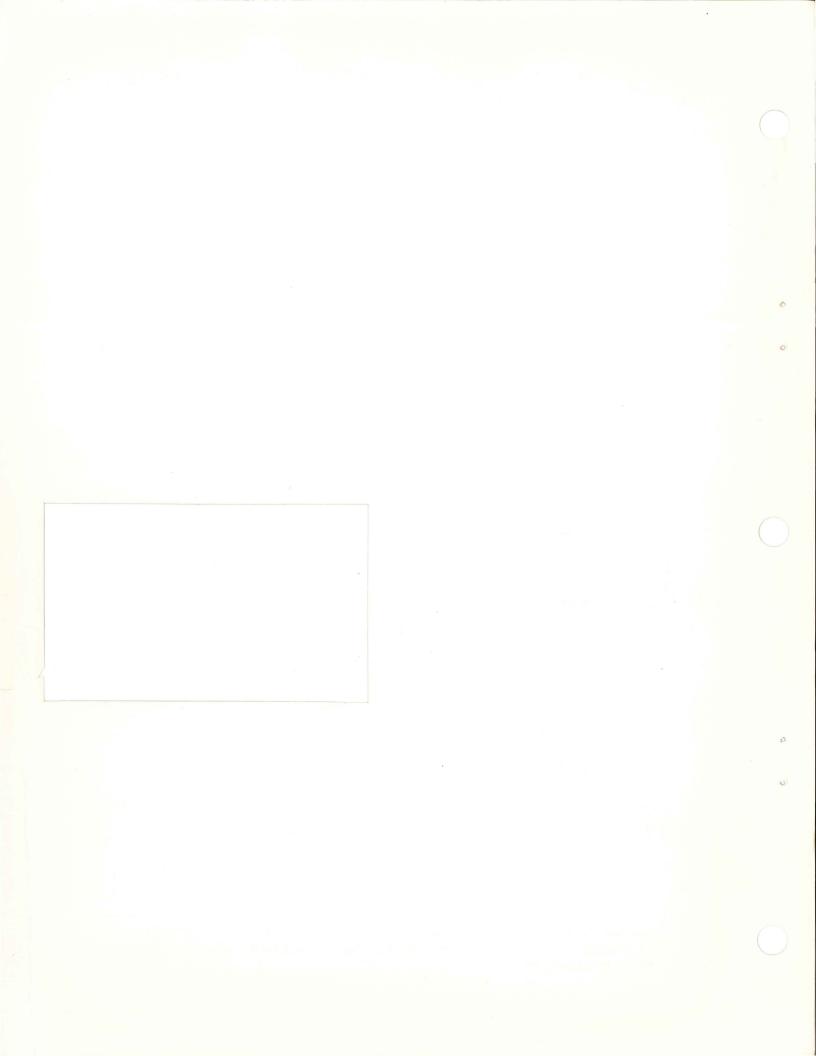
DDX900B TESTER

MAINTENANCE MANUAL

3310029-01

**Ampex Memory Products** 



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3310029-01

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### INTRODUCTION

This manual provides operating instructions and maintenance information for the Ampex DDX900B Tester. The DDX900B tester is used to test the DM900/9160-series and DM9000-series disk drives. This includes both single and dual-port disk drives.

Section I describes the physical characteristics of the tester and defines its operating controls and indicators.

Detailed instructions for connecting and operating the tester are given in section II.

Section III gives a functional description of the DDX900B circuit operation.

A complete set of maintenance diagrams, including schematics, assembly drawings, cable assemblies, and wire lists are provided in section IV.

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FIGURE 1-1. DDX900B TESTER

#### SECTION I

#### **GENERAL INFORMATION**

#### 1-1. INTRODUCTION

The Ampex DDX900B Tester, P/N 3309867-01, is a durable, lightweight, suitcase-type instrument (figure 1-1) that provides controls and signals necessary to exercise, align, and evaluate the performance of Ampex DM900/DM9160 and DM9000-series disk drives. Design of the tester permits a drive to be tested *off-line* without physically disconnecting any drive cables.

#### 1-2. PHYSICAL DESCRIPTION

The DDX900B is 17-3/4 inches long, 8-1/2 inches high, and 13-3/4 inches wide, and weighs approximately 24 pounds. A cable well on the right side of the tester provides storage for the interconnecting cables. All operator controls and indicators, except the AC POWER switch, are located on the front panel. The AC Power switch is located on the side of the chassis in the cable well. The top cover of the tester is removable and provides storage for the optional tools and accessories which are required to service each type of disk drive. These tools and accessories are listed in tables 1-1 and 1-2.

#### 1-3. Power Requirements

The tester has the following AC and DC power requirements.

- **a. AC Power.** The tester is wired in the factory to operate from either a 115 VAC, 50/60 Hz or 230 VAC, 50 Hz power source as specified by the customer. Units equipped for 115 VAC operation may be field-modified to operate from 230 VAC by replacing the 115 VAC fan (P/N 591-265) with a 230 VAC fan (P/N 591-220) and altering the power transformer wiring as follows:
  - (1) Remove 24-gage white wire from transformer lug AC2.
  - (2) Remove 24-gage black wire from transformer lug AC1.
  - (3) Connect both white and black wires to transformer lug D.
- **b. DC Power.** The tester has DC power requirements of  $\pm 15$  volts and  $\pm 5$  volts. The +5-volt logic power is provided by an internal 5-volt,  $\pm 5\%$  power supply. The other voltages,  $\pm 15$  VDC and -5 VDC, are supplied by the drive under test.
- c. Fuses. The power circuits of the tester are protected by a 1.5 ampere fuse that is located immediately below the POWER ON/OFF switch in the cable well.

#### 1-4. Cabling Requirements

Two cables, AC Power and Head Alignment, are permanently attached to the tester. One Double-Signal cable is provided with the tester. A Dual-Port Adapter and Signal cable are optional.

The Signal cable (P/N 3306288-01) provided with the tester is a double-ribbon-type cable assembly with two connectors on each end. One section has a 34-pin connector on each end and the other section has a 40-pin connector on each end. The Dual-Port Adapter cable (optional), P/N 3308359-01, is a single ribbon cable with a 20-pin connector on each end. The Dual-Port Adapter (optional), P/N 3307203-01, is a PCB assembly with three connectors (one 20-pin and two 34-pin). The Dual-Port Adapter and Dual-Port Adapter cable are used for the DM940, DM980, and DM9160 dual-port and convertible-to-dual-port drives.

TABLE 1-1. DM900/DM9160-SERIES OPTIONAL TOOLS AND ACCESSORIES

NOMENCLATURE	PART NO.
Head Alignment Tool	3306147-01
Head Mounting Tool	3306149-01
Torque-Limiting Screwdriver Handle	3302777-01
Head Torque Wrench Adapter	3306148-01
Dual-Port Adapter (TDPAD) PC Board*	3307203-01
Dual-Port Adapter Cable*	3308359-01
Card Extender	3307873-01

<sup>\*</sup> Required for use on CD and D ribbon cable drives.

TABLE 1-2. DM9000-SERIES OPTIONAL TOOLS AND ACCESSORIES

NOMENCLATURE	PART NO.
Initial Head Positioning Tool	3302377-01
Torque-Limiting (6 in./lbs) Screwdriver Assembly	3302778-01
Head-Spring Tensioner Tool	3302379-01
Head Installation and Adjustment Tool Assembly	3303728-01
Paddleboard (PDDL1)	3301883-01
Card Extender	3302153-01

#### NOTE

The Head Alignment cable should not be connected to the drive unless performing head alignment or servo balance adjustments.

#### 1-5. Electronic Components

All electronic components are mounted on the back of the front panel. Access is easily obtained by removing six screws and lifting the entire chassis out of the instrument case.

The tester logic chassis accommodates four printed circuit boards, but only three are used. A functional description of each PC board is provided in section III. Schematics and assembly drawings are included in section IV.

#### 1-6. Cooling

A muffin fan, located behind the front panel and adjacent to the power supply, provides cooling room air for the power supply and other electronic components. If the AC power requirements of the tester are modified, as described in paragraph 1-3a., the fan must also be changed.

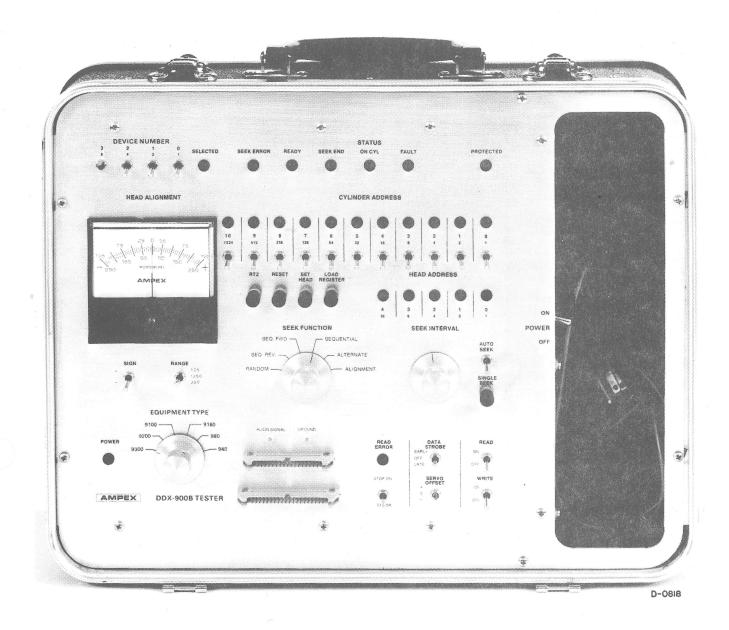


FIGURE 1-2. CONTROLS AND INDICATORS

### 1-7. OPERATOR CONTROLS AND INDICATORS

The operator controls and indicators (figure 1-2) consist of twenty-four toggle switches, five pushbutton switches, two rotary switches, one potentiometer, one zero nullmeter, and twenty-five light-emitting diode (LED) indicators. By following the operating instructions in section II, an operator can use the DDX900B to simulate control unit functions in testing and evaluating the performance of a disk drive. In response to the signals from the tester, the drive will return status signals which are displayed on the tester's LED indicators.

The controls and indicators are listed, and their operation is explained, in the following paragraphs.

#### 1-8. AC Power Switch and Indicator

This switch, when set to the ON (up) position, applies AC power to the tester. The AC POWER switch is located in the cable well. The POWER indicator is an LED that lights when the AC POWER switch is activated.

#### 1-9. Device Number Switches

The four DEVICE NUMBER switches (0, 1, 2, 3) are located on the upper left corner of the tester. These switches are binary coded to permit selection of the drive unit (0 through 15) under test. The unit address of the drive is determined by its module select identification plug.

#### 1-10. Status Indicators

The tester includes seven status lamps that indicate the operational condition of the drive under test.

- **a. Selected.** The SELECTED lamp lights to indicate that the unit address lines from the tester compare with the module select ID plug in the drive. When initiating tester operations, the SELECTED lamp will not light until one of the following switches are activated: RTZ, RESET, SET HEAD, SINGLE CYCLE, or AUTO SEEK. This action causes the Select Enable signal to the drive to go momentarily positive, thus satisfying the edge triggering requirement of the drive's select decode logic. If the addresses compare, the Selected line will activate within 250 nanoseconds after receipt of the leading edge of the Select Enable line.
- **b.** Seek Error. The SEEK ERROR lamp lights to indicate a seek incomplete condition in the drive. Seek incomplete will result if
  - (1) the drive fails to complete a seek within 100 ms.
  - (2) the drive fails to complete a head load rezero operation within 700 ms.
  - (3) the maximum address of the drive is exceeded.

The seek error condition can be cleared by pressing the RTZ pushbutton on the tester.

- **c. Ready.** The READY lamp lights to indicate that the selected drive is up to speed, heads are loaded, and no fault conditions exist.
- **d. Seek End.** The SEEK END lamp, when lit, indicates that a seek operation has terminated or a seek incomplete has occurred. The only time the SEEK END lamp will not be lit is when a normal seek is in progress.
- **e. On Cylinder.** The ON CYL lamp lights to indicate that a seek has been completed and the heads are positioned over a specified track.
- **f. Fault.** The FAULT lamp lights when a read/write unsafe condition is detected within the drive. This condition also causes the READY lamp to go out. The fault condition is cleared by pressing the RESET switch on the tester.
- **g. Protected.** The PROTECTED lamp, when lit, indicates that the READ-ONLY switch on the drive is on and the recording of information on the disk pack is inhibited.

#### 1-11. Cylinder Address Switches and Indicators

**a. Cylinder Address Switches.** The tester contains eleven CYLINDER ADDRESS switches (0 through 10). These switches are used to indicate the binary value of the cylinder (0 through 410 for DM940 and DM9100; 0 through 814 for DM9200 and DM9300; 0 through 822 for DM980; and 0 through 1644 for DM9160) to which the drives read/write heads are to be positioned during a seek operation. During sequential seeks, the CYLINDER ADDRESS switches can be set to indicate the desired seek increment (i.e., the number of

cylinders to be incremented during each subsequent seek). The switches are on when placed in the up position. The contents of the switches are loaded into the tester's internal cylinder address register/counter when the LOAD REGISTER button is pressed.

**b.** Cylinder Address Indicators. Associated with the CYLINDER ADDRESS switches are eleven LED indicators. Various combinations of these lamps are lighted during a seek cylinder operation (when the Set Cylinder tag is activated) to indicate the cylinder address on the bus lines to the drive.

#### 1-12. Head Address Switches and Indicators

- **a. Head Address Switches.** CYLINDER ADDRESS switches 0 through 4 also function as HEAD ADDRESS switches, and permit selection of heads 0 through 4 (DM900/DM9160 series) or heads 0 through 18 (DM9000 series). The contents of these five switches are loaded into the tester's head address register when the SET HEAD switch is pressed.
- **b. Head Address Indicators.** Associated with the HEAD ADDRESS switches are five LED indicators. Various combinations of these lamps are lighted during a seek head operation (when the Set Head tag is activated) to indicate the head address on the bus lines to the drive.

#### 1-13. Load Register Switch

This switch, when momentarily pressed, loads the contents of the CYLINDER ADDRESS switches into the cylinder address register/counter.

#### 1-14. Set Head Switch

When momentarily pressed, this switch loads the contents of the five HEAD ADDRESS switches into the head address register and starts the tester's seek sequencer. The seek sequence enables the Set Head tag, thus permitting the address in the head address register to be transferred to the drive via the bus lines.

#### 1-15. Reset Switch

The RESET switch, when momentarily pressed, causes the tester to transmit an Unsafe Reset signal (Control tag and bus bit 4 active) to the drive. This signal clears the fault (Read/Write Unsafe) condition in the drive and, as a result, the FAULT indicator on the tester will go out. Activation of the RESET switch also clears the tester's head address register, thus causing the HEAD ADDRESS indicators to go out.

#### 1-16. RTZ Switch

The RTZ switch, when momentarily pressed, causes the tester to send a Rezero signal (Control tag and bus bit 6 active) to the drive. This signal positions the heads to cylinder zero and turns off the SEEK ERROR lamp if it was lit due to a previous seek error.

#### 1-17. Seek Function Switch

The SEEK FUNCTION switch is a six-position rotary switch which provides control over the various seek operations. The switch positions are RANDOM, SEQ. REV., SEQ. FWD., SEQUENTIAL, ALTERNATE, and ALIGNMENT. The seek operations are described in section II.

#### 1-18. Seek Interval Potentiometer

This potentiometer permits the seek repetition rate to be increased or decreased when performing auto seeks.

#### 1-19. Auto Seek Switch

The ON (up) position of the AUTO SEEK switch permits seek operations to be continuously repeated.

#### NOTE

The READ and WRITE switches must be in the OFF position when performing auto seeks.

#### 1-20. Single Seek Switch

This pushbutton switch, when momentarily pressed, permits the drive to seek to the cylinder address in either the CYLINDER ADDRESS switches or in the cylinder address register/counter, depending on the type of seek function being performed.

#### 1-21. Equipment Type Switch

This six-position switch must be set to indicate the model number of the drive under test.

#### 1-22. Read/Write Switches and Indicators

The following switches and indicators are associated with read/write operations.

**a. Write Switch.** In the ON position, the WRITE switch permits the tester to write a random test pattern on the disk pack of the drive under test.

#### NOTE

The AUTO SEEK, STOP ON ERROR, and READ switches must be OFF when performing a write operation.

**b. Read Switch.** This switch, when ON, permits the tester to read a data test pattern which was previously recorded on a disk pack using the write capabilities of the tester.

#### NOTE

The AUTO SEEK and WRITE switches must be OFF when performing a read operation.

- c. Read Error Indicator. This LED lights if a read data error is detected during a read operation.
- d. **Stop On Error Switch**. If this switch is ON (up) and a read data error is detected, the READ ERROR lamp will light and the read operation will be halted. This switch must be in the OFF (down) position during a write operation.
- **e. Data Strobe Switch.** This switch is used during a read operation to time-shift the read data through the data separator in the drive. The EARLY position causes the data separator to strobe the read data at a time earlier than normal. The LATE position causes the data separator to strobe the data at a time later than normal. When the switch is in the OFF position, operation of the data separator is not affected.

**f. Servo Offset Switch.** If an error is detected during a read operation, this switch permits the heads to be repositioned so that the read operation can be retried, thus permitting the recovery of hard to read data. The + position causes the heads to be moved a fixed distance off the center of the track (toward the pack center). The — position causes the heads to be moved a fixed distance off the center of the track (away from the pack center).

#### 1-23. Head Alignment Meter, Sign and Range Switches

The HEAD ALIGNMENT meter is a null-balance meter that is required for servo balance and head alignment procedures. The SIGN and RANGE switches control the operation of the meter. Instructions for operation of the meter are provided in section II, paragraphs 2-14 and 2-15.

#### **SECTION II**

#### **OPERATION**

#### 2-1. DDX900B TESTER INITIAL CHECKOUT PROCEDURE

The DDX900B Tester is completely checked out in the factory prior to shipment. However, to ensure that the tester is operating normally, it is recommended that the following simple checkout procedure be performed before initially connecting the tester to a disk drive.

- a. Set all toggle switches, including the AC POWER switch, to the OFF, or down, position. (The AC POWER switch is located in the cable well.)
- b. Connect the AC power cord to an appropriate AC voltage source (115 VAC, 60 Hz or 230 VAC, 50 Hz, depending on the power requirements of the tester).
  - c. Set AC POWER switch ON (up position) and verify that POWER indicator lamp is lighted.
  - d. Set SEEK FUNCTION switch to ALTERNATE position.
- e. Press RESET, RTZ, SET HEAD, LOAD REGISTER, and SINGLE SEEK buttons and verify that all indicator lamps, except POWER, are out.
  - f. Set CYLINDER ADDRESS bit 0 switch ON (up position).
  - g. Press SINGLE SEEK button and verify that CYLINDER ADDRESS bit 0 indicator lamp lights.
  - h. Press SINGLE SEEK button again and verify that the indicator lamp goes out.
  - i. Repeat steps f. through h. for cylinder address bits 1 through 10.
- j. Set EQUIPMENT TYPE, SEEK FUNCTION and CYLINDER ADDRESS switches in the sequence shown in table 2-1. Perform the three seek functions for all models as follows.

#### (1) SEQUENTIAL

- (a) Press LOAD REGISTER button momentarily to load cylinder address previously entered from table 2-1.
- (b) Set all CYLINDER ADDRESS switches to the OFF (down) position, and set the CYLINDER ADDRESS bit 0 switch to the ON (up) position.
- (c) While repeatedly pressing the SINGLE SEEK button, verify that the CYLINDER ADDRESS indicator lamps advance up to maximum cylinder address (table 2-1), and then start decrementing in one-cylinder increments.

#### (2) SEQUENTIAL FORWARD

- (a) Press LOAD REGISTER button momentarily to load cylinder address previously entered from table 2-1.
- (b) Set all CYLINDER ADDRESS switches to the OFF (down) position, and set the CYLINDER ADDRESS bit 0 switch to the ON (up) position.

TABLE 2-1. FUNCTION TEST DATA

EQUIPMENT TYPE	SEEK FUNCTION	CYLINDER ADDRESS (MAXIMUM)	CYLINDER ADDRESS	CYLINDER ADDRESS BITS
	SEQUENTIAL		400	8, 7, 4
DM940	SEQ. FWD.	410	400	8, 7, 4
	SEQ. REV.		8 .	3
	SEQUENTIAL		800	9, 8, 5
DM980	SEQ. FWD.	822	800	9, 8, 5
	SEQ. REV.		8	3
	SEQUENTIAL		1632	10, 9, 6, 5
DM9160	SEQ. FWD.	1644	1632	10, 9, 6, 5
	SEQ. REV.		8	3
	SEQUENTIAL		400	8, 7, 4
DM9100	SEQ. FWD.	410	400	8, 7, 4
	SEQ. REV.		8	3
	SEQUENTIAL		800	9, 8, 5
DM9200	SEQ. FWD.	814	800	9, 8, 5
	SEQ. REV.		8	3
	SEQUENTIAL		800	9, 8, 5
DM9300	SEQ. FWD.	814	800	9, 8, 5
	SEQ. REV.		8	3

<sup>(</sup>c) Repeatedly press the SINGLE SEEK button until CYLINDER ADDRESS indicators indicate maximum cylinder address (table 2-1), then reset to cylinder address 0 (does not decrement), and again start advancing in one-cylinder increments.

#### (3) SEQUENTIAL REVERSE

- (a) Press LOAD REGISTER button momentarily to load cylinder address previously entered from table 2-1.
- (b) Set all CYLINDER ADDRESS switches to the OFF (down) position, and set the CYLINDER ADDRESS bit 0 to the ON (up) position.

- (c) Repeatedly press the SINGLE SEEK button until CYLINDER ADDRESS indicators indicate cylinder address 1, next indicates maximum cylinder address (table 2-1), and then decrement in one-cylinder increments.
  - k. Set all toggle switches (except AC POWER) to OFF position.
  - I. Set SEEK FUNCTION switch to ALIGNMENT position.
  - m. Set EQUIPMENT TYPE switch to 9100, 9200, or 9300 position.
- n. While repeatedly pressing and releasing the SET HEAD button, verify that the HEAD ADDRESS indicator lamps sequence from 0 through 18, and then return to 0.
- o. Set EQUIPMENT TYPE switch to 940, 980, or 9160 position and repeat step n., only this time, verify that the HEAD ADDRESS indicator lamps sequence from 0 through 4, and then return to 0.
  - p. Set AC POWER switch and all other toggle switches to the OFF position.

#### 2-2. DISK DRIVE PREPARATION AND TESTER CONNECTION

Prior to initiating any tester functions, the drive must be connected to the tester and prepared for operation. The following paragraphs define this procedure for both the DM900/DM9160 and DM9000-series disk drives.

#### 2-3. DM940, DM980, or DM9160 Preparation

- a. Stop the drive and wait for pack to stop rotating.
- b. Set AC POWER switch on DDX900B tester to OFF.
- c. Turn off main power circuit breaker CB1 on drive.
- d. Remove customer disk pack and install scratch pack (or CE pack if head alignment is required).
- e. Remove the top cover assembly.
- f. When testing a basic disk drive (DM940 and DM980 only), connect Cable Assembly, P/N 3306288-01, as follows (figure 2-1):
- (1) Connect the 34-wire ribbon cable from connector J1 (DDX900B) to the edge connector on the A01 PCB in the drive.
- (2) Connect the 40-wire ribbon cable from connector J2 (DDX900B) to the edge connector on the A02 PCB in the drive.
- g. When testing a DM940, DM980, or DM9160 convertible-to-dual-port (CD) or dual-port (D) disk drive, connect Dual-Port Adapter (TDPAD), P/N 3307203-01, Dual-Port Adapter Cable, P/N 3308359-01, and Cable Assembly, P/N 3306288-01, as follows (figure 2-2):
  - (1) Connect the dual-port adapter connector J3 to the DDX900B tester J1.
- (2) Connect the 34-wire ribbon cable from the dual-port adapter connector J2 to the edge connector J1 on the AO1 PCB in the drive.
- (3) Connect the 20-wire ribbon cable from the dual-port adapter connector J1 to the edge connector J1 (port A) on the AO3 PCB in the drive (convertible-to-dual-port (CD) and dual-port (D) disk drives). In order to test port B on a dual-

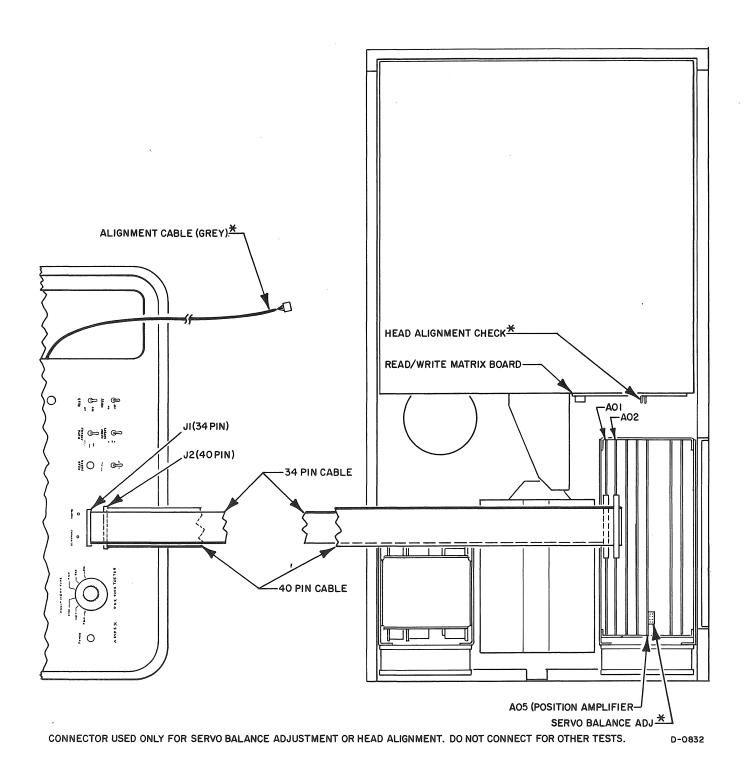


FIGURE 2-1. DM900-SERIES/TESTER CABLE CONNECTIONS (BASIC)

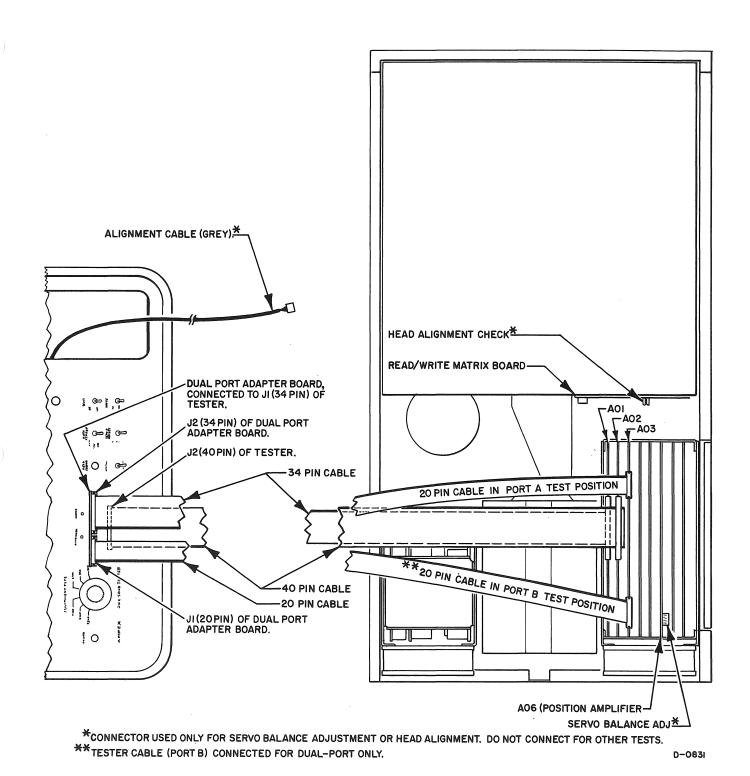


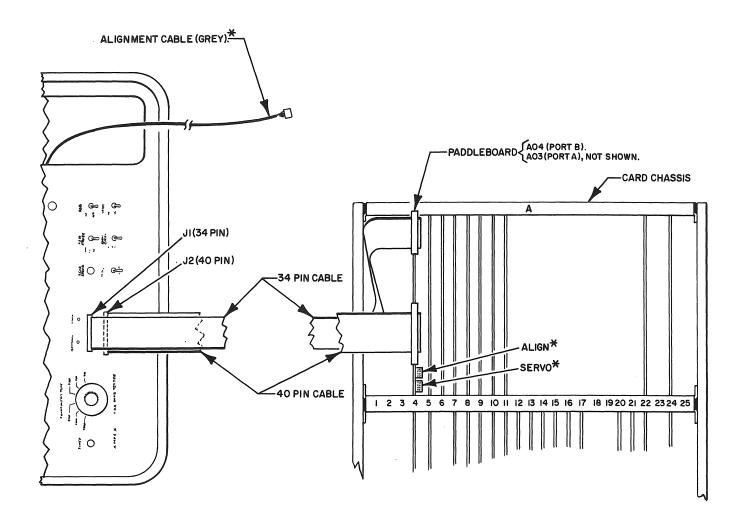
FIGURE 2-2. DM900/9160-SERIES/TESTER CABLE CONNECTIONS (CD AND D VERSIONS)

port drive, the 20-wire ribbon cable (same cable as in previous step) must be removed from edge connector J1 (port A) on the AO3 PCB and inserted in edge connector J2.

- (4) Connect the 40-wire ribbon cable from connector J2 (DDX900B) to the edge connector J1 on the A02 PCB in the drive.
- h. Set the address of the drive under test into the four DEVICE NUMBER switches located on the upper left corner of the tester.
  - i. Verify that AUTO SEEK, READ, and WRITE switches on DDX900B are off.
  - j. Select DM940, DM980, or DM9160 switch position on DDX900B.
  - k. Set AC POWER switch on tester to ON (up) position.
  - I. Set main power circuit breaker CB1 on drive to ON.
  - m. Start disk drive.
  - n. Press RESET switch on DDX900B tester.
  - o. Verify that SELECTED, READY, and SEEK END indicator lamps are lit and all other status indicators are off.

#### 2-4. DM9100, DM9200 or DM9300 Preparation (Figure 2-3)

- a. Stop drive and wait for pack to stop rotating.
- b. Set AC POWER switch on DDX900B to OFF.
- c. Turn off main power circuit breaker CB1 on drive.
- d. Remove customer disk pack and install scratch pack (or CE pack if head alignment is to be performed).
- e. When testing a basic DM9000-series disk drive, connect Cable Assembly, P/N 3306288-01, and install Paddleboard, P/N 3301883-01, as follows (figure 2-3):
  - (1) Install paddleboard in the AO4 PCB location in the drive.
- (2) Connect the 34-wire ribbon cable from connector J1 (DDX900B) to the 34-pin edge connector on the paddleboard.
- (3) Connect the 40-wire ribbon cable from connector J2 (DDX900B) to the 40-pin edge connector on the paddleboard.
- f. When testing a DM9000CD-series (convertible-to-dual-port) disk drive, connect Cable Assembly, P/N 3306288-01, and install Paddleboard, P/N 3301883-01, as follows (figure 2-3):
  - (1) Install paddleboard in the AO3 PCB location in the drive (not shown in figure 2-3).
- (2) Connect the 34-wire ribbon cable from connector J1 (DDX900B) to the 34-pin edge connector on the paddleboard.
- (3) Connect the 40-wire ribbon cable from connector J2 (DDX900B) to the 40-pin edge connector on the paddleboard.



CONNECTOR USED ONLY FOR SERVO BALANCE ADJUSTMENT OR HEAD ALIGNMENT. DO NOT CONNECT FOR OTHER TESTS.

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#### FIGURE 2-3. DM9000-SERIES/TESTER CABLE CONNECTIONS

- g. When testing a DM9000D-series (dual-port) disk drive, connect Cable Assembly, P/N 3306288-01, and install Paddleboard, P/N 3301833-01, as follows (figure 2-3):
  - (1) Install paddleboard in the AO3 (port A) or AO4 (port B) PCB location in the drive.
- (2) Connect the 34-wire ribbon cable from connector J1 (DDX900B) to the 34-pin edge connector on the paddleboard.
- (3) Connect the 40-wire ribbon cable from connector J2 (DDX900B) to the 40-pin edge connector on the paddleboard.
- h. Set the address of the drive under test into the four DEVICE NUMBER switches located on the upper left corner of the tester.
  - i. Verify that AUTO SEEK, READ, and WRITE switches on DDX900B are off.
  - j. Set EQUIPMENT TYPE switch to model under test (DM9100, DM9200, or DM9300).

- k. Set AC POWER switch on DDX900B to ON (up) position.
- I. Set circuit breaker CB1 on drive to ON.
- m. Start disk drive.
- n. Press RESET switch on tester.
- o. Verify that SELECTED, READY, and SEEK END indicator lamps are lit and all other status indicators are off.

#### 2-5. SEEK OPERATIONS

The type of seek is selected by the SEEK FUNCTION switch. The seek operations are explained in the following paragraphs.

#### 2-6. Alternate Seeks

- a. Set SEEK FUNCTION switch to ALTERNATE. (Internal cylinder address register/counter will reset to zero.)
- b. Set CYLINDER ADDRESS switches to first desired cylinder address.
- c. Press LOAD REGISTER switch to transfer switch contents to the internal cylinder address register/counter.
- d. Set the CYLINDER ADDRESS switches to second desired cylinder address.
- e. If single cycle operation is desired, press SINGLE SEEK switch. The drive will seek to the cylinder address in the switches or in the internal cylinder address register/counter. The next time SINGLE SEEK is pressed, the drive will seek to the other address. These steps are repeated each time SINGLE SEEK is pressed.
- f. If automatic operation is desired, set AUTO SEEK switch ON. With this switch on, the alternate seeks will be continuously repeated. The frequency (repetition rate) of the seeks can be controlled by the SEEK INTERVAL potentiometer.

#### 2-7. Sequential Seeks

- a. Set SEEK FUNCTION switch to SEQUENTIAL. (Internal cylinder address register/counter will reset to zero.)
- b. If desired, a starting cylinder address can be set into the CYLINDER ADDRESS switches and entered into the internal cylinder address register/counter by pressing LOAD REGISTER. Otherwise, the sequential seek will start at cylinder zero.
- c. Set CYLINDER ADDRESS switches for desired cylinder seek increment (e.g., if switch 1 (binary 2) is on and all others off, the drive seek increment will be two cylinders at a time).
- d. If single cycle operation is desired, the drive will sequentially seek the specified number of cylinders each time SINGLE SEEK is pressed.
- e. If automatic operation is desired, set AUTO SEEK switch ON. Assuming the CYLINDER ADDRESS switches contain the desired cylinder seek increment (e.g., two cylinders), the drive will automatically seek forward two cylinders at a time until maximum cylinder is detected, and will then seek in reverse two cylinders at a time until cylinder O is detected. The sequential forward and reverse seeks will be continuously repeated until the AUTO SEEK switch is turned off.

#### 2-8. Sequence Forward

a. Set SEEK FUNCTION switch to SEQ. FWD. (Internal cylinder address register/counter will reset to zero.)

- b. The Sequence Forward operation is identical to the Sequential Seek operation, with the exception that when the maximum cylinder is reached, the heads will return directly to cylinder address zero rather than decrementing.
  - c. Sequence Forward can be performed in SINGLE SEEK or AUTO SEEK modes.

#### 2-9. Sequence Reverse

- a. Set SEEK FUNCTION switch to SEQ. REV. (Internal cylinder address register/counter is preset to maximum cylinder address.)
- b. The Sequence Reverse operation is identical to the Sequential Seek operation, except that the seek will start from the maximum cylinder address (or the address specified in the internal register) and decrement the specified number of cylinders in the reverse direction until cylinder 1 (not 0) is reached. The heads will then return directly to the maximum cylinder address.
  - c. Sequence Reverse can be performed in SINGLE SEEK or AUTO SEEK modes.

#### 2-10. Random Seeks

- a. Set SEEK FUNCTION switch to RANDOM.
- b. For single cycle operation, the drive will seek to any random legal cylinder each time the SINGLE SEEK switch is pressed.
- c. If automatic operation is desired, set AUTO SEEK switch ON. The drive will continuously seek to different random legal cylinders until the switch is turned off.

#### 2-11. READ/WRITE OPERATIONS

The tester is capable of writing or reading a unique test pattern on a disk pack.

When either the read or write operations are performed, all seek functions are also operable. The AUTO SEEK switch and the SINGLE SEEK switch must not be activted when the READ or WRITE switches are in the ON position.

If the SEEK FUNCTION switch is in any seek position except ALTERNATE, a write or read will be performed on all tracks (head selection will be automatically incremented) before seeking to the next cylinder. With the switch in the ALTERNATE position, only the selected head will be used.

#### 2-12. Write Operation

#### **CAUTION**

Before initiating a write operation, install a scratch pack on the drive; otherwise, customer data will be destroyed.

- a. Set SEEK FUNCTION switch to desired seek position.
- b. Start write operation by setting WRITE switch to ON position. (STOP ON ERROR switch must be off.)
- c. The tester will write a pseudo-random pattern, starting with the cylinder and head address of a particular track, which is repetitive every 65,535 bits.

#### 2-13. Read Operation

Data written during the write test can be verified during the read operation.

- a. Set SEEK FUNCTION switch to desired seek position.
- b. Set READ switch to ON position.
- c. If the STOP ON ERROR switch is on, the read operation will halt if an error is detected and the READ ERROR indicator will light. If the switch is off, the READ ERROR indicator will flash, but the read operation will not stop.
- d. If a read error is detected, the SERVO OFFSET switch can be placed in the + or positions, and the read operation can be retried.
- e. The DATA STROBE (EARLY or LATE) switch provides a means of shifting the data through the drive's data separator, earlier or later than normal.

#### 2-14. SERVO BALANCE ADJUSTMENT

The servo balance adjustment must be performed precisely for proper head alignment. This balance must be checked prior to head alignment and adjusted if error is greater than 25 microinches for DM900-series, DM9000-series, or DM9160 disk drives. Replacing the position amplifier assembly A05 (DM940 and DM980 drives), A06 (DM940D, DM940CD, DM980D, DM980CD, and DM9160 disk drives), servo position assembly B20 (DM9100, DM9200, and DM9300 drives), or a component thereon, could necessitate adjusting the servo balance. Perform the adjustment as follows.

- a. Stop drive and turn off main power CB1.
- b. Install CE pack on drive and turn on READ-ONLY switch.
- c. Connect DDX900B alignment (grey) cable to drive as follows:
  - (1) On DM940/DM980 or DM9160 drives, connect to receptacle on position amplifier circuit board.
  - (2) On DM9100, DM9200, or DM9300, connect to SERVO connector on paddleboard.

#### NOTE

The DDX900B tester should already be connected to the drive and set up as described in paragraphs 2-3e. through 2-3k. or paragraphs 2-4e. through 2-4k.

- d. Set SEEK FUNCTION switch on tester to ALIGN position.
- e. Set appropriate alignment track (245 for DM940, DM980, DM9160, or DM9100 drives; 496 for DM9200 or DM9300 drives) into the DDX900B CYLINDER ADDRESS switches.

64)

- f. Turn on main power circuit breaker CB1 and start drive.
- g. Press SINGLE SEEK on tester (drive will seek to specified alignment track).
- h. Toggle the SIGN switch between the + and positions while, at the same time, observing the HEAD ALIGNMENT meter for a *null* condition (not necessarily zero).

i. If a *null* condition is not indicated, calculate the error, using equation in paragraph 2-15, step p. If the error is greater than 25 microinches, adjust the BALANCE ADJUST potentiometer on position amplifier assembly for DM940, DM980, and DM9160 drives, and servo position assembly for DM9100, DM9200, and DM9300 drives, so that the meter reading is the same (null) for both positions of the switch.

#### 2-15. HEAD ALIGNMENT PROCEDURE

- a. Stop drive and turn off main power circuit breaker CB1.
- b. Install CE pack on drive and turn on READ-ONLY switch.

#### CAUTION

The CE pack should have been in the same room environment as the drive for 2 hours before mounting on the drive. The drive should then run a minimum of 1 hour to temperature-stabilize the pack and drive before head alignment is checked or performed. When head alignment is being performed on more than one drive, the CE pack requires only a 15 minute stabilization if (1) the pack was taken immediately from the previous drive, and (2) the drive under test has been operating with heads loaded for a minimum of 60 minutes preceding the test.

#### NOTE

The servo balance must be precisely adjusted to ensure proper head alignment. Check the servo balance adjustment, paragraph 2-14, before continuing with this head alignment procedure.

- c. Connect DDX900B alignment (grey) cable to drive as follows:
- (1) On DM940, DM980, and DM9160, connect to head alignment receptacle on read/write matrix circuit board.
  - (2) On DM9100, DM9200, or DM9300, connect to ALIGN connector on paddleboard.

#### NOTE

- The tester should already be connected to the drive as explained in paragraphs 2-3e. through 2-3k. or paragraphs 2-4e. through 2-4k.
- d. Set SEEK FUNCTION switch on tester to ALIGN position.
- e. Set appropriate alignment track (245 for DM940, DM980, DM9160, or DM9100 drives; 496 for DM9200 or DM9300 drives) into the tester CYLINDER ADDRESS switches.
  - f. Turn on main power circuit breaker CB1 and start drive.
  - g. Press SINGLE SEEK on the tester (drive will seek to specified alignment track).

h. Press RESET switch, then repeatedly press the SET HEAD switch until the desired head number (usually zero) is indicated by the HEAD ADDRESS lamps.

#### NOTE

The selected head (usually zero) is now reading the alignment track. A servo track, identical to those on the servo disk, is recorded on all surfaces of the CE pack at cylinder 245 or 496 with a "guardband" on each side of the alignment cylinder. The dibit pattern can be observed by connecting an oscilloscope to the ALIGN SIGNAL test point on the DDX900B.

If monitored with an oscilloscope, the read head signal would appear like the servo head signal. The head is properly aligned when its plus peak amplitude is equal to its minus peak amplitude.

i. Place the RANGE switch on the tester to the 1250 position.

#### NOTE

The head alignment area consists of a blank area, an outer guardband of minus even servo pulses, the alignment cylinder, an inner guardband of plus odd servo pulses, and an inner blank area. If a read/write head is far enough off track to be in the blank area, the meter will be in a null position as if the head were perfectly aligned. It must be assured the meter null is from on-track condition and not from the head being in a blank area.

- j. With the head torque wrench, loosen the head holding screw and reset to 40 inch-ounces (2.5 inch-pounds).
- k. Insert the alignment tool into the holes in the T-bar and head mounting block.
- I. Move the head arm as far as it will go back toward the T-bar. Then move the head arm forward (toward the center of the pack) and watch the HEAD ALIGNMENT meter on the tester for the following sequence:
- (1) The meter reading will peak negative as the head starts reading the outer guardband of the alignment area when the SIGN switch is in the + position.
  - (2) The meter reading will null (pass through zero) as the head passes exact alignment track location.
  - (3) The meter reading will peak positive as the head enters the inner guardband of the alignment area.
  - (4) The meter reading will drop to zero as the head passes from the inner guardband to the blank area.

The above sequence must be followed to assure proper alignment.

- m. Again, with the alignment tool, move the head back (away from the spindle), watching the meter reading peak positive, then drop toward zero.
- n. As the meter reading decreases and approaches zero, keep switching the RANGE switch until it is on the minimum (125) range.

o. With the RANGE switch in the 125 position, use the head alignment tool and move the head so that by toggling the + or - SIGN switch, the meter reads the same for each position of the SIGN switch.

#### NOTE

Perfect head alignment may not occur at a "zero" meter reading. Each tester will have its own inherent "DC offset." The SIGN switch is a means of determining the DC offset for a given tester. The head will be in alignment when the meter reads the same for both positions of the SIGN switch. Once the DC offset is determined for a given tester, all other heads may be adjusted to the same meter reading without regard to the SIGN switch. The amount of offset is typically less than 25 microinches.

p. Calculate head alignment error using the following equation. If the error is greater than 15 microinches for DM9160, 25 microinches for DM980, DM9200, or DM9300, 50 microinches for DM940 or DM9100 disk drives, repeat steps i. and k. through p.

Alignment Error (Microinches) = 
$$\frac{\text{(Positive Meter Reading)} - \text{(Negative Meter Reading)}}{X}$$

UNIT	940	980	9160	9100	9200	9300
X	2	4	8	2	4	4

#### **EXAMPLE**

Disk Drive	DM9100
+Meter Reading	75
-Meter Reading	100

ERROR = 
$$\frac{75 - (-100)}{2} = \frac{175}{2} = 87.5$$
 microinches

- q. Tighten the head holding screw to 80 inch-ounces (5 inch-pounds) of torque.
- r. Check the HEAD ALIGNMENT meter to be sure tightening the screw did not move the head. If the head has moved out of alignment, as specified in step p., loosen the screw and repeat steps o. thru r.
- s. Press the SET HEAD switch to advance the head address register contents so the next head may be aligned. Repeat steps i. thru r. until all heads have been aligned.
- t. Perform data burst check (paragraph 2-16, steps b. through i) if a read/write head or the servo head is replaced. Perform only on DM940, DM980, or DM9160 disk drives (all versions).

- u. Set appropriate alignment track (245 for DM940, DM980, DM9160, or DM9100 drives; 496 for DM9200 or DM9300 drives) into the tester CYLINDER ADDRESS switches.
  - v. Set SEEK FUNCTION switch to ALTERNATE position.
- w. Set the AUTO SEEK switch on and SEEK INTERVAL fully clockwise (fast). Let the drive seek between cylinders 0 and 245 for 5 minutes.
  - x. Set AUTO SEEK switch off.
  - y. Perform head alignment check.
- z. Repeat steps o. through y. (except step t.) if the error on any head is greater than 30 microinches for DM9160, 50 microinches for DM980, DM9200, or DM9300, 75 microinches for DM940 or DM9100 disk drives.

#### 2-16. DATA BURST CHECK (DM940, DM980, or DM9160, ALL VERSIONS)

The data burst check must be performed whenever a read/write head or the servo head is replaced.

- a. Perform steps a. through d., paragraph 2-15.
- b. Set CYLINDER ADDRESS switches to cylinder 10 and press SINGLE SEEK switch.
- c. Connect the oscilloscope to the ALIGN SIGNAL test point on the tester panel.
- d. Sync the oscilloscope on the positive edge of the index pulse, TP1 on the Pack Control/Index (AO2) printed circuit board.
  - e. The first pulse of data must be 4 microseconds  $\pm 2$  microseconds from the sync point.
  - f. Press the SET HEAD switch to advance the head address register contents so the next head may be checked.
  - g. If any of the heads do not meet the specification in step e., the head must be replaced.
  - h. If all the heads do not meet the specification in step e., replace the servo head.
  - i. Repeat steps c. through k. for cylinders 200 and 300.

#### Craxafqiffig microscom (1995) saft mariyit (2 om U. 1997, SECTION III oʻli in colora caracha teologi.

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#### 3-1. GENERAL

The electronic functions of the DDX900B Tester are performed by three printed circuit boards. The location, nomenclature, and schematic drawing number of each PC board is as follows:

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. Providence de la companya de la c	Seek Logic (SEEKL)	3307973-01
	Pattern Write/Read (PRLOG)	3307983-01
	Head Alignment (HDALN)	3305710-01

Schematic and assembly drawings of the tester PC boards are provided in section IV. These drawings should be referenced throughout the following discussion.

# 3-2. SEEK LOGIC — A01 has safe particular to be a permit that a province of the control of the c

The seek logic consists of the cylinder address register/counter, a 5-MHz crystal oscillator, maximum cylinder detection circuitry, a sequence skip counter, latches for various front panel switches, seek sequencer logic, and miscellaneous control and gating networks.

The cylinder address register/counter is shown on A01, Sht. 2. This circuit consists of three type-191 synchronous 4-bit up/down binary counter integrated circuits (IC's). Two data multiplexers, each consisting of three type-157 IC's, are associated with the address register/counter. The A inputs to both sets of multiplexer chips are supplied from the CYLINDER ADDRESS switches SB00 through SB10. Switches SB00 through SB04 also function as the head address switches, and SB00 through SB07 function as inputs to the sequence skip counter (A01, Sht. 1). The B inputs to multiplexer 1 represent the maximum cylinder address. The B inputs to multiplexer 2 are the outputs of the cylinder address register/counter.

### 3-3. Initial Power Application

Operation of the two data multiplexers and the cylinder address register/counter is controlled by the circuits on AO1, Sht. 1. When power is first applied, multiplexer 1 is either cleared (to all zeros) or preset (to the maximum cylinder address), depending upon the position of the SEEK FUNCTION switch. Flip-flop F/F1, the clear/preset control flip-flop, is forced high when the switch is in the ALT., SEQUENTIAL, SEQ. FWD., or RANDOM positions, thus conditioning the clear (+CLR) AND-gate. If the switch is in the SEQ. REV. position, F/F1 is forced clear and conditions the preset (+PRESET) AND-gate. The power-up condition causes the output of a 250-nanosecond one-shot to go high and activates either the clear or preset signals, depending on which output gate is conditioned by F/F1. The output of the 250-nanosecond one-shot also activates the load (-LOAD) signal which loads the output of the multiplexer 1 into the cylinder address register/counter. Thus, the cylinder address register/counter is either cleared to zero or preset to the maximum cylinder address when power is first applied.

At the same time, multiplexer 2 is inhibited (all outputs go low) by the —ENABLE LINE signal from the seek sequencer. This line does not become active until the seek sequence (A01, Sht. 3) is running. Operation of the seek sequencer is explained in paragraph 3-5. The reset condition of multiplexer 2 clears the bus-out lines (connector J1) and the lines to the cylinder register (CYLAO through CYLA10).

#### 3-4. Seek Operation

When the LOAD REGISTER switch is pressed, the contents of the CYLINDER ADDRESS switches are loaded from multiplexer 1 into the cylinder address register/counter. The counter is clocked on the low-to-high transition of the advance count pulse; however, this signal is not generated until the seek sequencer is operating. The output of the counter is provided to the

B inputs of multiplexer 2 and to the maximum cylinder detection circuit (AO1, Sht. 1). When the +REG input to multiplexer 2 is high, the B inputs are enabled, permitting the address from the cylinder address register/counter to be transferred to the multiplexer. However, when the +REG signal goes low, the A inputs (directly from the switch latches) are enabled. This later condition occurs only when SET HEAD is pressed, the SEEK FUNCTION switch is in ALTERNATE, or head alignment is being performed. The +REG signal is controlled by flip-flop F/F2 on AO1, Sht. 1. The outputs of multiplexer 2 are transferred to the bus-out lines when the seek sequencer activates the -ENABLE LINE.

**3-5. SEEK SEQUENCER.** Before any operations can be performed on the drive, the drive must indicate that it is selected by lighting the SELECTED indicator on the tester. In order to accomplish this, the seek sequencer (AO1, Sht. 3) must be started. The select enable (—SELE) output signal (AO1, 3A1) to the drive is normally active (low); however, the internal selection logic circuits of the drive are designed for edge triggering. Therefore, anyone of the following switches must be activated: RTZ, RESET, SET HEAD, SINGLE SEEK, or AUTO SEEK. This clocks the seek control F/F (AO1, 3A5) and permits the type-93 four-bit binary counter to start counting clock pulses at a 5-MHz rate. These clock pulses are provided by crystal oscillator Y1 (AO1, Sht. 1). The counter outputs are decoded by a type-42 BCD-to-decimal decoder. (See the seek sequencer timing diagram in figure 3-1.) The third clock pulse causes the select enable (—SELE) signal to go high for 2OO-nanoseconds. The negative-going edge of this signal triggers the selection circuit in the drive. If the drive's address matches the address set into the four unit address switches on the tester, the drive responds with a signal that lights the SELECTED indicator on the tester.

The seek sequencer is activated any time a seek or reset operation is performed. The outputs of the BCD-to-decimal decoder control two flip-flops. The enable F/F conditions and provides sufficient settling time for three translation logic AND-gates. One of these gates activates the —ENABLE LINE which permits the outputs from multiplexer 2 (AO1, Sht. 1) to be placed on the bus-out lines to the drive. The tag F/F conditions the three tag line output gates, and permits one of the tag signals (set head, set cylinder, or control tag) to be activated, depending upon the operation being performed. (Table 3-1 defines the functions of the bus-out lines for each of the three tag line signals.) For example, during a cylinder seek, the —SET CYL TAG could be activated by pressing the SINGLE SEEK switch, by placing the AUTO SEEK switch on, or by receiving a —CYL SEEK signal from the read/write cylinder seek logic (AO2, Sht. 3). The entire seek sequence is repeated for each seek operation.

- **3-6. MAXIMUM CYLINDER DETECTION.** The maximum cylinder detector circuit is shown on the left side of AO1, Sht. 1. Its purpose is to detect when the maximum cylinder address is in the cylinder address register/counter. With the SEEK FUNCTION switch in any position except ALIGNMENT or ALTERNATE, detection of the maximum cylinder address triggers the 250-nanosecond one-shot which causes the cylinder address register/counter to be either cleared or preset to the maximum address. For example, if the SEEK FUNCTION switch is in the SEQ. FWD. position, the cylinder address register/counter is reset to all zeros when maximum cylinder is detected, and if the switch is in the SEQ. REV. position, the counter is preset to the maximum allowable cylinder address. It should be noted that the purpose of the maximum cylinder detector is not to detect address errors (i.e., addresses higher than maximum) since circuits for that specific purpose are included in each disk drive.
- 3-7. **SEQUENCE SKIP COUNTER.** The sequence skip counter (AO1, Sht. 1) consists of two 4-bit synchronous down-counter IC's connected in cascade. Its purpose is to advance the cylinder address register/counter the number of cylinders set into the CYLINDER ADDRESS switches each time a seek is performed. The sequence skip counter is required for forward seeks, reverse seeks, and sequential seeks, but not for alternate or random seeks. If the SEEK FUNCTION switch is in any of the sequence positions, the skip counter is loaded with the contents of the CYLINDER ADDRESS switches (bits 0 through 7) whenever the seek sequencer (AO1, Sht. 3) sets the enable F/F (AO1, 3B3). This action activates the +ENABLE LINE signal which is ANDed with -SET HD and -ALT to cause the LD inputs to the skip counter IC's to go low (active). When +ENABLE LINE drops, the 5-MHz clock pulses count down the skip counter, causing a +ADV COUNT pulse to advance the cylinder address register/counter once for each down count. As an example, if CYLINDER ADDRESS switches 0 and 1 (binary 3) are on, and the SEEK FUNCTION switch is in the SEQ. FWD. position, the cylinder address register/counter will be advanced three times, and the new cylinder address will be strobed onto the bus-out lines when the sequencer again activates the enable signals. If the AUTO SEEK switch is on, the advance sequencer will continue until maximum cylinder is detected, at which time the cylinder address register/counter is cleared and the advance sequence is repeated, starting from cylinder 0 and progressing forward in three-cylinder increments.

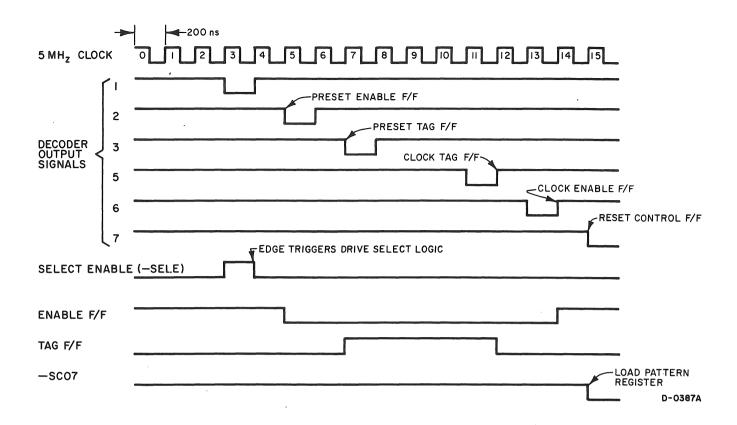


FIGURE 3-1. SEEK SEQUENCER TIMING DIAGRAM

TABLE 3-1. FUNCTION TAG/BUS-OUT DEFINITIONS

BUS-OUT	SET CYLINDER TAG	SET HEAD TAG	SET CONTROL TAG
0	Cylinder Address 1	Head Select 1	Write Select
1	Cylinder Address 2	Head Select 2	Read Select
. 2	Cylinder Address 4	Head Select 4	Offset Forward
3	Cylinder Address 8	Head Select 8	Offset Reverse
4	Cylinder Address 16	Head Select 16	Unsafe Reset
5	Cylinder Address 32		Address Mark
6	Cylinder Address 64		Rezero
7	Cylinder Address 128		Data Strobe Early
8	Cylinder Address 256		Data Strobe Late
9	Cylinder Address 512*		Release Command (Dual-Port)
10	Cylinder Address 1024**		

<sup>\*</sup> Not used on DM940

<sup>\*\*</sup> For DM9160 only

If the SEEK FUNCTION switch is set to SEQ. REV., but all other switch settings remain as in the previous example, the cylinder address register/counter will be preset to the maximum cylinder address and then decremented downward in three-cylinder increments. With the switch set to the SEQUENTIAL position, the cylinder address register/counter is advanced from 0 to maximum cylinder address in three-cylinder increments, and then decremented back to cylinder address 0 in three-cylinder increments.

#### 3-8. READ/WRITE LOGIC — A02

The read/write logic consists of the servo clock (bit) counter, the head register, the cylinder register, the pattern generator, and read/write control logic.

#### 3-9. Servo Clock Counter

The servo clock counter (AO2, Sht. 1) provides the necessary timing for all tester read/write sequences. The counter is driven by servo clock signals from the drive. The servo clock signal (+SCDL) is returned to the drive as the write clock signal (AO2, 2B1). If the STOP ON ERROR switch is on and a read error is detected, the —HALT signal will inhibit counter operation. Times translated by the servo clock counter are provided to the read/write control logic (AO2, Sht. 3).

#### 3-10. Read/Write Control

Before a read or write operation can be performed with the tester, the disk drive heads must be positioned to a desired cylinder and a specific head must be selected. The cylinder seek, head seek, and read/write operations are described in the following paragraphs.

- **3-11. CYLINDER SEEK.** All functions of the read/write control logic (AO2, Sht. 3) are initiated by the receipt of an index (—INDEX) signal from the drive. If the READ or WRITE switches are on, the drive is selected and on cylinder, and there are no error conditions, the D input to F/F3 will go high and the flip-flop will be clocked by the index pulse. The Q output (high) of F/F3 is ANDed with the  $\overline{Q}$  (high) output of F/F4 to generate the —CYL SEEK signal. This signal goes to the seek control logic (AO1, 3C8) and starts the seek sequencer. The sequencer activates the —SET CYL TAG signal, allowing the drive heads to be positioned to the cylinder address that is stored in the cylinder address register/counter or CYLINDER ADDRESS switches. The selected and on-cylinder signal (+SEON) will momentarily glitch (go low) during the seek operation.
- **3-12. HEAD SEEK.** When the heads are positioned on cylinder, signal +SEON will go high and toggle F/F4. The set state of this flip-flop causes the -CYL SEEK signal to deactivate (go high) and makes the D input to F/F5 high. The next index pulse clocks F/F5, resulting in a high D input to F/F6. Flip-flop F/F6 is clocked by the +16 output signal from the servo clock counter and causes the seek head signal (-SEEK HD) to go active (low). The -SEEK HD signal turns on the seek sequencer (A01, Sht. 3), and when the sequencer tag F/F sets, causes the -SET HD TAG signal to be sent to the drive. At this same time, the +SEEK HD signal (A02, 1B8) clocks the head register, enabling its outputs to be placed on bus lines 0 through 4 via the line drivers on A01, Sht. 2. The desired head number should have been previously loaded into the head register by setting the appropriate HEAD ADDRESS switches and pressing the SET HEAD switch. Thus, a cylinder seek has been completed, a head has been selected, and the drive is now ready for the read or write operation.
- **3-13. READ SEQUENCE.** Assuming that a servo offset is not being performed (i.e., SERVO OFFSET switch is in 0 position), flip-flops F/F7 and F/F8 are clocked at time +64. If the READ switch is in the ON position, this action activates the -RD GATE signal and the read/write control (-R/W CON) signal. The -R/W CON signal deactivates the -SEEK HD signal and activates the -CONTROL TAG signal (A01, 3D1) to the drive.

At time +286, flip-flop F/F9 is clocked and activates the +ENABLE SEARCH signal. The high state of this signal releases the force clear input to flip-flop F/F11, permitting the flip-flop to search for the first "one-bit" transition (sync pulse) occurring on the +NRZ DATA IN line. The sync pulse sets the flip-flop, causing the +ENABLE RD SHIFT signal to go high. This signal functions as the shift clock signal for the pattern generator (AO2, Sht. 2) and initiates the regeneration of the data pattern for comparison with the incoming read data.

**3-14. PATTERN GENERATION.** The pattern generator (AO2, Sht. 2) is a 16-bit shift register that is loaded with the contents of the head register and the cylinder register when seek sequencer activates signal —SCO7, indicating that the seek sequence is complete. The pin 5 input to the pattern generator IC, on the extreme right (AO2, 2B3), represents the sync bit. Going from right to left, the next five input lines to the pattern generator IC's are from the head register, and the next ten input lines are from the cylinder register. Thus, the starting (or home) address of the pattern generator will always be different, depending on which head and cylinder is selected.

Four output signals from the pattern generator (pins 10, 11, 12, and 13) are exclusively ORed (A02, 2A3), resulting in a pseudo-random bit pattern that is fed back to the input of the pattern generator and is serially shifted through the register by the shift clock signal. This pattern is repeated every 65,535 bits.

The serial data output (pin 10) of the pattern generator shift register is exclusively ORed (AO2, 2A4) with the read data from the drive. If the incoming data does not compare with the data pattern, the D input to the read error detect flip-flop goes high, and the flip-flop is clocked by the next read clock signal. This condition lights the READ ERROR indicator and, if the STOP ON ERROR switch is on (up), halts the operation of the servo clock counter (AO2, Sht. 1). It should be noted that the data pattern read from the disk must previously have been written using the tester's write capability.

- **3-15. READ DETECTION.** Two circuits that have not yet been mentioned are the read clock detect one-shot (AO2, 2A6) and the NRZ detect one-shot (AO2, 2A5). The purpose of these one-shots is to detect the total absense of read clock or read data signals from the drive during a read operation.
- **3-16. WRITE SEQUENCE.** The write data operation is performed in much the same manner as the read, except the pattern generation is shifted by the +ENABLE WRITE SHIFT signal (WRITE switch must be on) from F/F10. This signal also gates the serial write data pattern to the drive via the write data line driver (AO2, 2B2).
- **3-17. SERVO OFFSET.** When the SERVO OFFSET switch is in the + or positions, flip-flop F/F7 is enabled and flip-flop F/F8 is disabled. Flip-flop F/F7 is clocked at time +64 and provides a high D input to flip-flop F/F12. Flip-flop F/F12 is clocked by the next index pulse; however, the read and write gates are inhibited by the low Q output of flip-flop F/F8. These gates remain inhibited until the next +64 pulse from the servo clock counter toggles flip-flop F/F8. Thus, the servo offset operation effectively disables the read or write capability for one complete revolution of the disk pack, while allowing time for offsetting the position of the heads.

### 3-18. HEAD ALIGNMENT — A03

The head alignment PC board is used only for aligning the read/write heads of a disk drive and is not required for any of the other tester functions. The head alignment circuitry includes three stages of AGC amplification, a phase-lock oscillator (PLO) frequency comparator, two peak detector circuits, a difference (error) amplifier, a summation amplifier, and a meter calibration circuit. A simplified block diagram is shown in figure 3-2. The designations in the bottom of the blocks (e.g., U3, U6, etc.) represent the IC's as shown on the head alignment schematic diagram.

# 3-19. AGC Amplification

The input stage to the head alignment PC board is a dual differential amplifier (U3) with a gain of approximately one. This amplifier receives a 200-millivolt differential signal (HEAD-A and HEAD-B) from the selected read/write head. If the head is perfectly aligned, the signal will be the balanced dibit pattern (measured at the ALIGN terminal of the tester) shown in figure 3-3(A). If the head is misaligned, the dibit pattern will resemble the waveforms of figure 3-3(B) or 3-3(C).

The dibit pattern is developed as follows. A track, approximately 0.015 inch wide (identical to that prerecorded on the servo disk), is recorded on each side of the alignment cylinders (245 or 496) on all surfaces of the CE disk pack. The recorded bits on these tracks are called dibits. The dibits are polarized opposite for adjacent tracks, such that even track dibits start out negative and odd track dibits start out positive. When the read/write head is perfectly aligned over an alignment cylinder, it will be astride two of these prerecorded tracks. In this position, the head will see even and odd track dibits equally, producing the balanced dibit pattern shown in figure 3-3(A). If the head is misaligned toward the center of the pack, the dibit pattern will be distorted as shown in figure 3-3(B), and if the head is misaligned away from the center of the pack, the dibit pattern will be distorted as shown in figure 3-3(C).

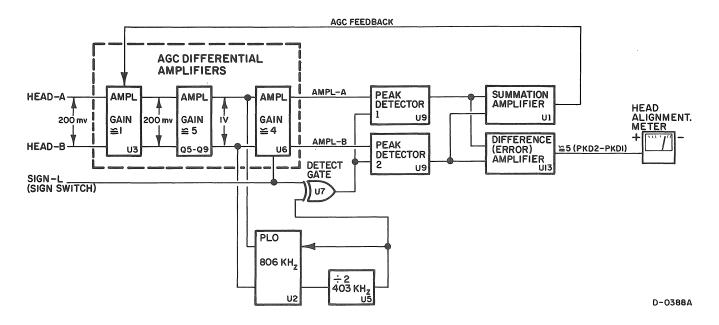


FIGURE 3-2. HEAD ALIGNMENT CIRCUIT, SIMPLIFIED BLOCK DIAGRAM

The operation of amplifier U3 is controlled by the AGC feedback signal from summation amplifier U1. The summation amplifier compares the outputs of peak detectors 1 and 2. The head is considered to be accurately aligned and reading a balanced dibit signal if the DC averages of the two peak detectors equal zero. However, if the difference is not zero, the output of the summation amplifier will go more positive or more negative, depending upon the direction of misalignment.

The output of the first stage amplifier U3 is provided to another differential amplifier stage with a gain of approximately 5. The emitter follower outputs of this amplifier are fed to dual differential amplifier U6 and to phase-lock oscillator U2.

Amplifier U6 operates as either an inverting or a noninverting amplifier, depending on whether the head is misaligned in the direction of an even or an odd track. The inverting/noninverting function is controlled by the SIGN switch. The outputs of amplifier U6 (signals AMPL-A and AMPL-B) are provided to peak detectors 1 and 2, respectively. The operation of the peak detector circuits is explained in paragraph 3-21.

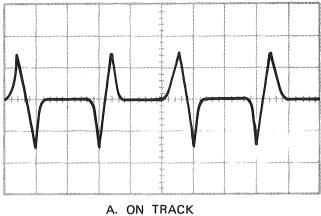
## 3-20. Frequency Comparator

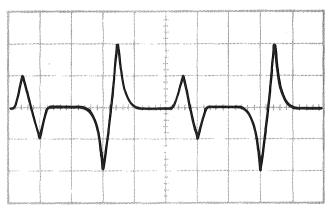
As previously stated, the outputs from the second stage of amplification are also provided to phase-lock oscillator (PLO) U2 which operates as a frequency comparator. With no input signals present, the oscillator free-runs at a frequency of approximately 806 kHz. However, when input signals are present, the oscillator frequency is locked up at two times the frequency of the incoming signals. Two flip-flops (U5) divide the PLO frequency by two and return the 1/2 F signal to the oscillator for comparison with the incoming frequency.

The resulting stabilized squarewave signal from the divide-by-two flip-flop is exclusively ORed (U7) and generates Detect Gate signal DTGT-L which is fed to the peak detector circuits. Operation of exclusive OR-gate U7 is controlled by the SIGN switch on the tester's front panel.

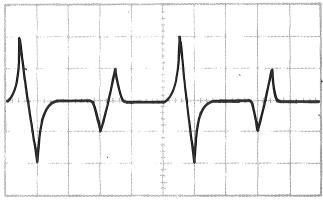
#### 3-21. Peak Detection Circuits

The peak detector circuits are shown on AO3, Sht. 2. The upper half of dual differential amplifier U9 monitors the positive-going peaks of amplifier signal AMPL-A, and the lower half monitors the positive-going peaks of amplifier signal AMPL-B. The Detect Gate signal (DTGT-L) functions as an electronic switch to alternately sample the two peak detector circuits. The detect gate is a squarewave whose negative transition turns off peak detector 2 and turns on peak detector 1, and whose positive transition turns off peak detector 1 and turns on peak detector 2.





B. OFFSET TOWARDS PACK CENTER



C. OFFSET AWAY FROM PACK CENTER

D-0346

FIGURE 3-3. HEAD ALIGNMENT DIBIT PATTERN

Following is an example of how the peak detector operates. Assume that peak detector 1 is active. The positive-going peak of the input signal causes U9 pin 4 to go more positive than U9 pin 3. This turns on the left transistor. Its collector, U9 pin 1, goes negative and turns on transistor Q2. Capacitor C4 rapidly charges, placing a positive voltage at TP4. When the voltage at U9 pin 3 reaches its positive peak, the right transistor turns on and the left transistor turns off, preventing C4 from any further charge. However, the positive voltage developed across C4 remains until peak detector 1 is again sampled. Peak detector 2 is sampled in an identical manner when the detect gate squarewave goes positive.

The peak detector output signals (PKD1-A and PKD2-A) are fed to pin 2 of summation amplifier U1 (A03, Sht. 1). The voltage at the summing junction is held at a fixed level by the setting of AMPLITUDE ADJ. potentiometer R15.

## 3-22. Error Amplifier

The error amplifier (U13) compares the positive voltage from peak detector 1 with the negative voltage (inverted by U12) from peak detector 2. The difference is amplified approximately five times and fed through fixed-gain amplifier U15 to the head alignment meter. Thus, if the difference between the peak detectors is zero, the head alignment should indicate a zero or balance condition when the SIGN switch is toggled back and forth. This means that the head is perfectly balanced. However, if the head is misaligned, the difference between the peak detectors will be indicated by the deflection of the head alignment meter.

#### 3-23. Internal Calibrator

The internal calibrator circuit provides a means of adjusting the head alignment PCB. Detailed checkout and adjustment instructions are provided in paragraph 3-24. The calibrator circuit is shown on the upper part of A03, Sht. 2. It is not included in the block diagram of figure 3-2 since it is not a functional part of the head alignment circuit.

The main calibrator circuits are oscillator U8, synchronous counter U10, BCD-to-decimal decoder U11, transistors Q12 through Q15, and differential amplifier U14. The oscillator drives counter U10 and is adjusted for an output frequency of exactly 403 kHz at U10 pin 6. The output states of the counter are decoded by BCD-to-decimal decoder U11. The decoder outputs are gated on the negative transitions of the 403 kHz signal and turn on either transistor Q13 or Q15. Transistor Q12 is a constant-current generator for these transistors. Normally, the current path from Q12 is through Q14 to ground. However, if either Q13 or Q15 are on, the current flows through R101 or R100 to ground and develops a small input voltage on differential amplifier U14 pins 1 and 2. This differential signal is amplified by U14 and sent to pins 7 and 3 of the calibration connector.

When performing calibration adjustments to the head alignment PCB, the grey head alignment cable must be plugged into the calibration connector.

#### 3-24. CHECKOUT AND ADJUSTMENT OF HEAD ALIGNMENT PCB

The head alignment PCB is precisely adjusted and checked out in the factory prior to shipment and should not require adjustment during normal operation. However, the following procedure should be performed if the head alignment PCB is replaced, or if any components are changed on the board or in the meter circuit.

- a. Turn off AC POWER switch.
- b. Place head alignment board in card extender and insert extender into PCB location A03.
- c. Turn AC POWER switch on.
- d. Check out and, if necessary, adjust the internal calibration oscillator circuit as follows:
  - (1) Place a jumper wire (short) between TP1 and TP2.
  - Connect oscilloscope probe to TP9.

(3) Adjust R85, as required, until oscilloscope indicates a frequency of exactly 403 kHz.

#### NOTE

If components have been changed, it may be necessary to select new capacitors C24 and C25, and then readjust R85 until a precise frequency of 403 kHz is obtained.

- (4) Remove jumper wire between TP1 and TP2.
- e. Adjust PLO frequency comparator U2 as follows:
  - (1) Connect oscilloscope to inverter U4 pin 4.
  - (2) Verify that oscilloscope indicates a frequency of 806 kHz  $\pm 2$  kHz.

## **NOTE**

If frequency is not within tolerance, select new capacitors C54 and C55 until correct tolerance is obtained.

- f. Perform balance and amplitude adjustments and meter calibration as follows:
  - (1) Connect jumper wires from TP1 to TP2, TP13 to TP14, and TP7 to ground.
  - (2) Set RANGE switch on tester to 1250 position.
  - (3) Plug head alignment (grey) cable into alignment connector on head alignment PCB.
  - (4) Connect digital voltmeter (DVM) to TP10.
- (5) While observing the DVM, toggle the SIGN switch between its + and positions, and adjust R62 (BALANCE ADJ.) until the positive and negative millivolt readings are the same.
  - (6) Remove jumper between TP7 and ground.
- (7) While observing the DVM, toggle the SIGN switch between  $\pm$  and  $\pm$  positions, and adjust R15 (AMPLITUDE ADJ.) until the positive and negative readings indicate  $\pm$ 10 volts and  $\pm$ 10 volts, respectively, with a maximum allowable tolerance of  $\pm$ 150 millivolts. If this tolerance cannot be obtained, R62 in step (5) may be readjusted away from the original positive and negative readings by  $\pm$ 35 millivolts.
- (8) Adjust R91 (METER CAL.) for maximum + and full-scale meter reading while toggling the SIGN switch between its + and positions.
  - (9) Connect jumper wire between TP7 and ground.
  - (10) Repeat steps (5) through (8) to eliminate the possibility of circuit interaction.
- (11) Disconnect DVM from TP10, remove all jumper wires, turn AC POWER switch off, remove head alignment PCB from card extender, and install the PCB in card location AO3.

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# **SECTION IV**

# **MAINTENANCE DIAGRAMS**

### 4-1. GENERAL

This section provides maintenance personnel with a complete set of maintenance diagrams for the Ampex DDX900B Tester. Included are schematic and assembly drawings of the printed circuit board assemblies, an overall assembly drawing of the tester, together with its related parts list, all applicable interconnecting cable drawings, and internal wire lists.

## 4-2. LOGIC SYMBOLOGY

The logic symbols used on the schematic diagrams are specified in MIL-STD-806B. Standard definitions are used and active levels are listed on all input and output lines.

## 4-3. LIST OF DRAWINGS

### **SCHEMATIC DIAGRAMS**

Title	Location	Drawing No.
Seek Logic (SEEKL)	A02	3307970-01 3307980-01 3305710-01 3307200-01
Dual-Port Tester Adaptor (TDPAD) +5 V Power Supply		3307200-01

# **ASSEMBLY DRAWINGS AND PARTS LIST**

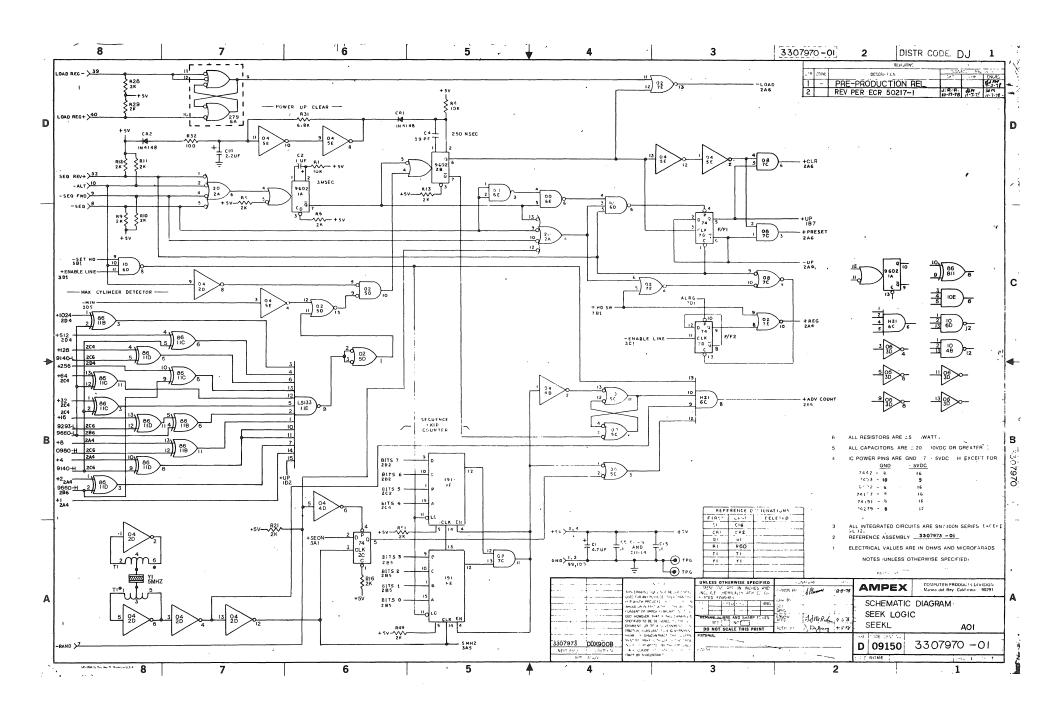
Title	Drawing No.
Paddleboard (PDDL1)	3301883-01 3305713-01 3307203-01 3307973-01 3307983-01 3309867-XX
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### **INTERCONNECTING CABLE ASSEMBLIES**

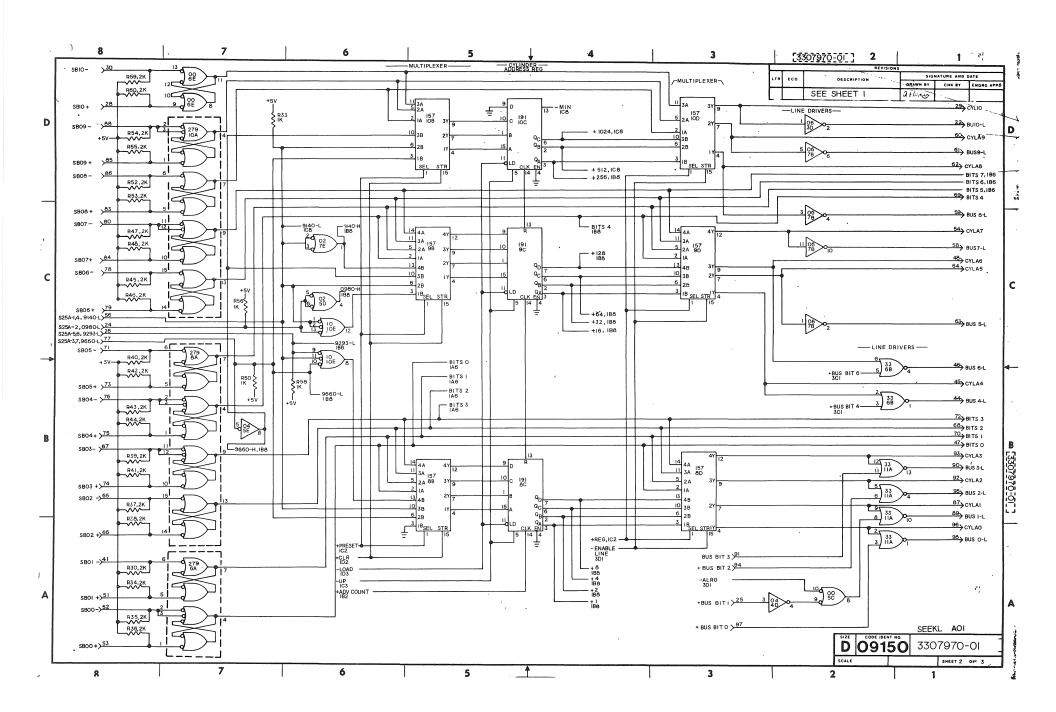
Title	Drawing No.
Cable Assembly	3306288-01
Head Alignment Cable Assembly	3306365-01
Dual-Port Adapter Cable Assembly	3308359-01

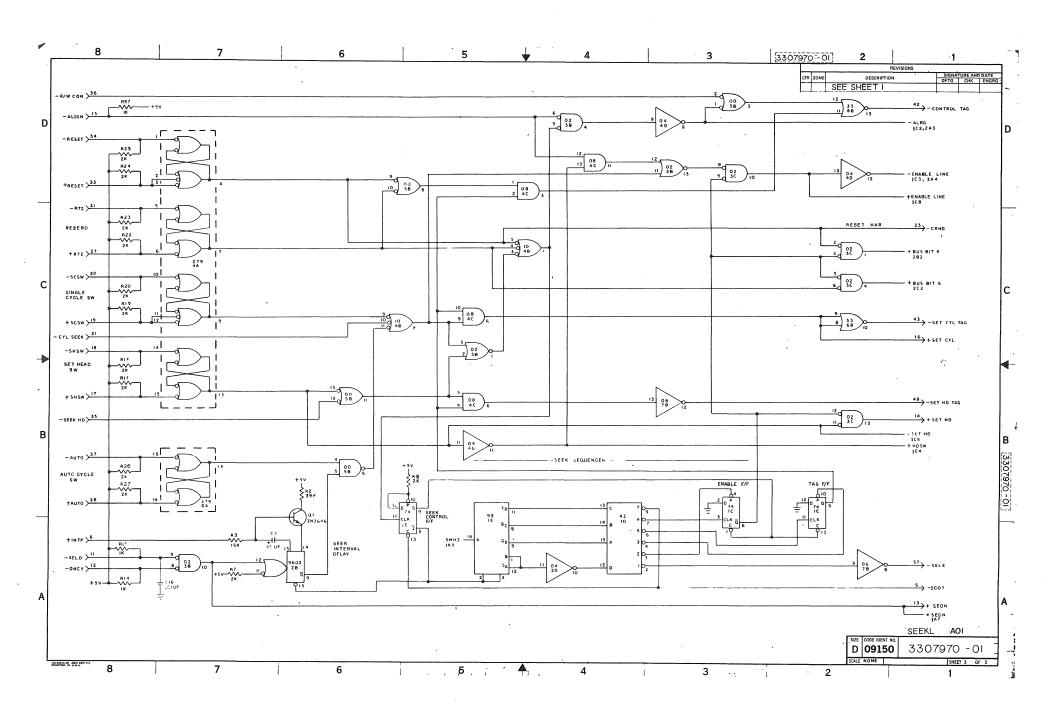
# **INTERNAL WIRE LISTS**

Title	Drawing No.
J2 to Logic Chassis	3303826-01
AC and DC Power	
Control Panel Wiring	3309875-01
J1 to Logic Chassis	3309876-01
Logic Chassis Wiring	3310017-01

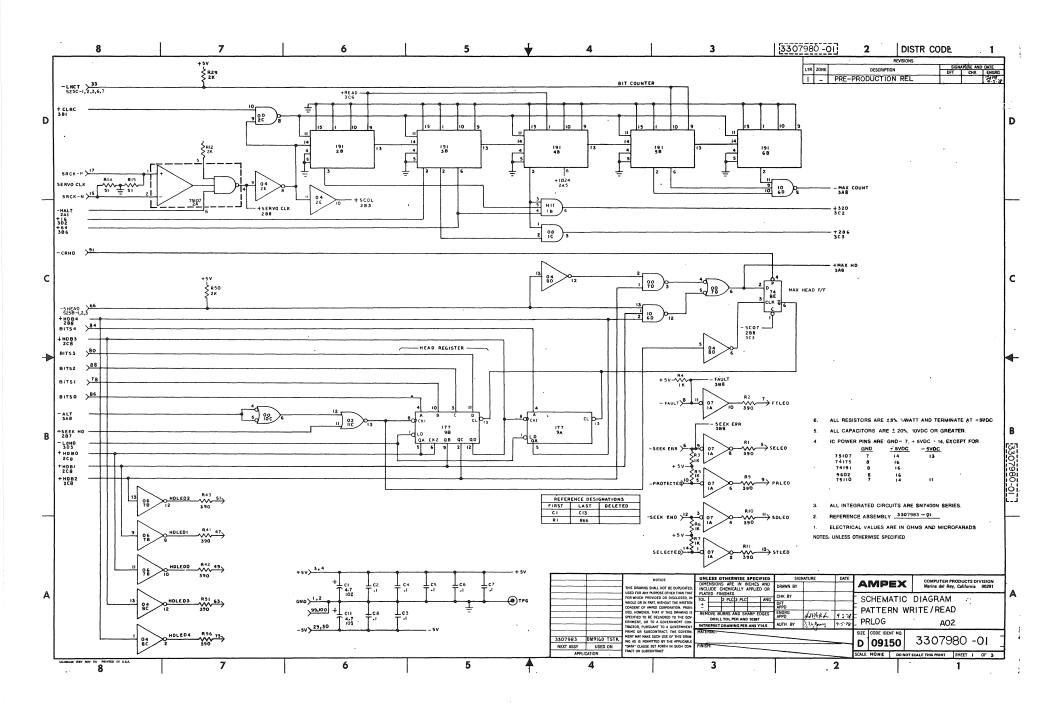


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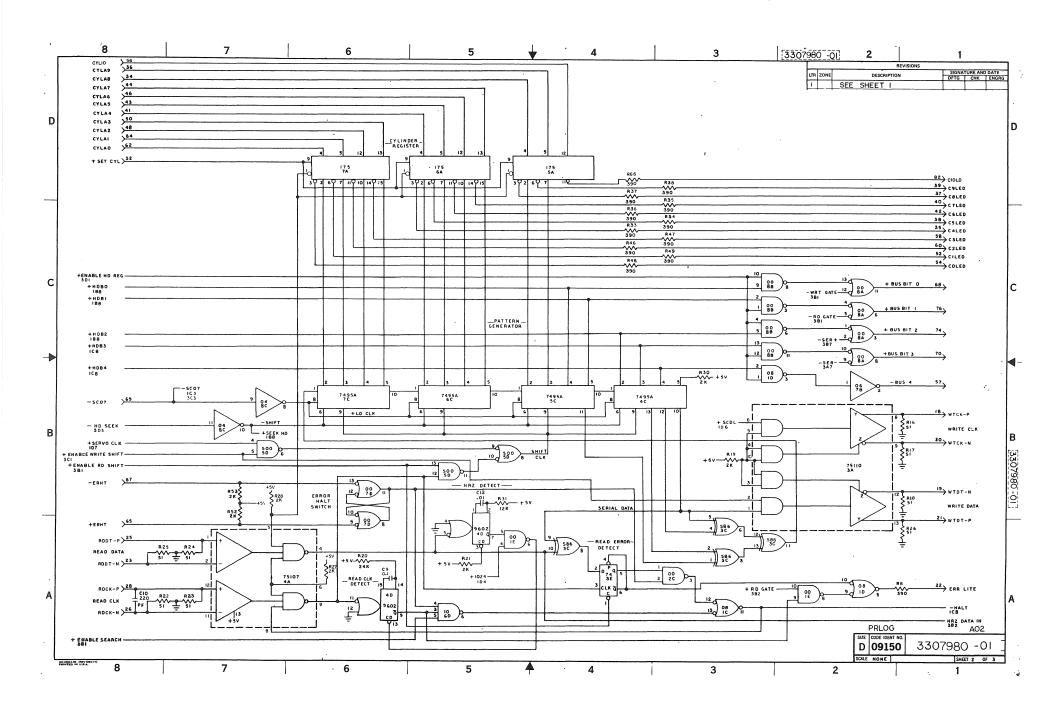


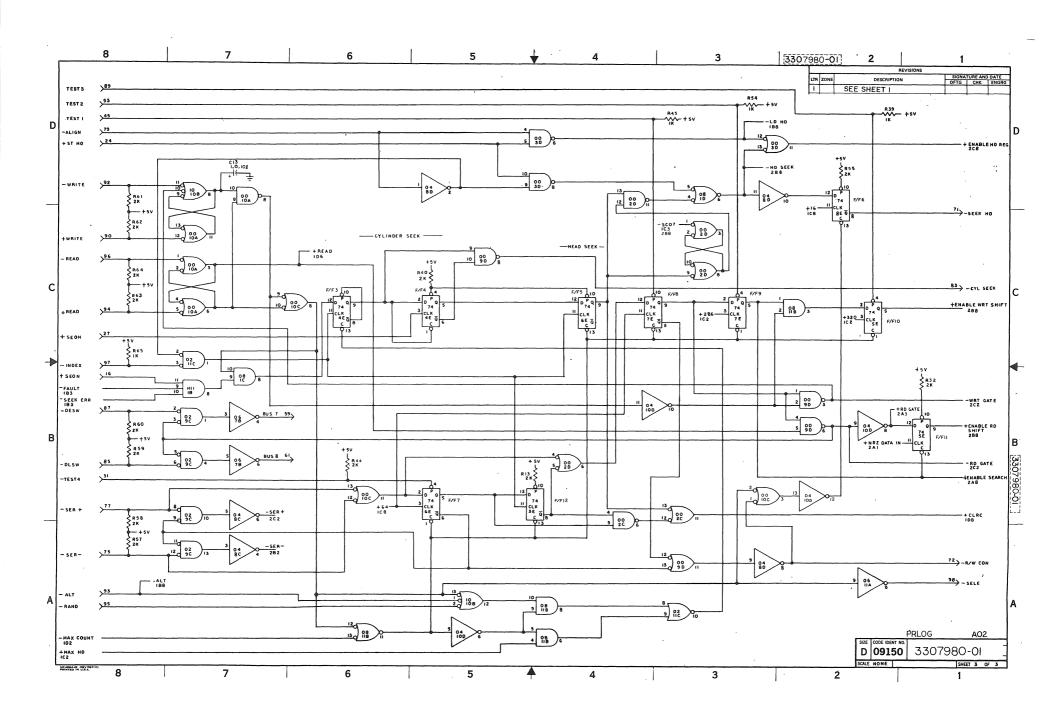


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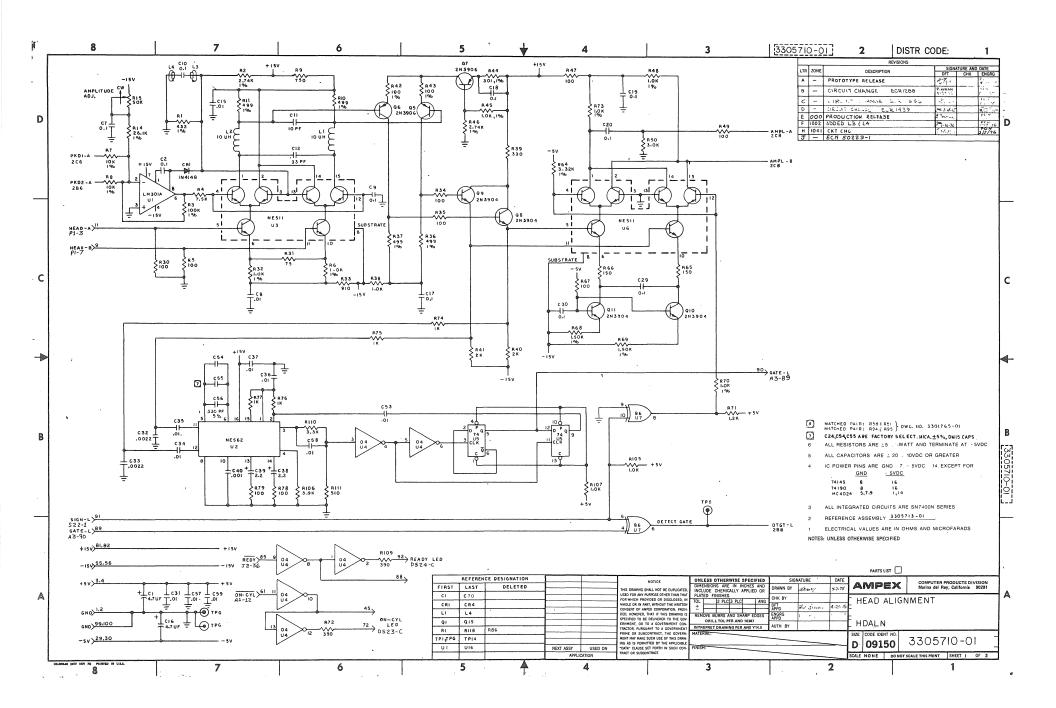


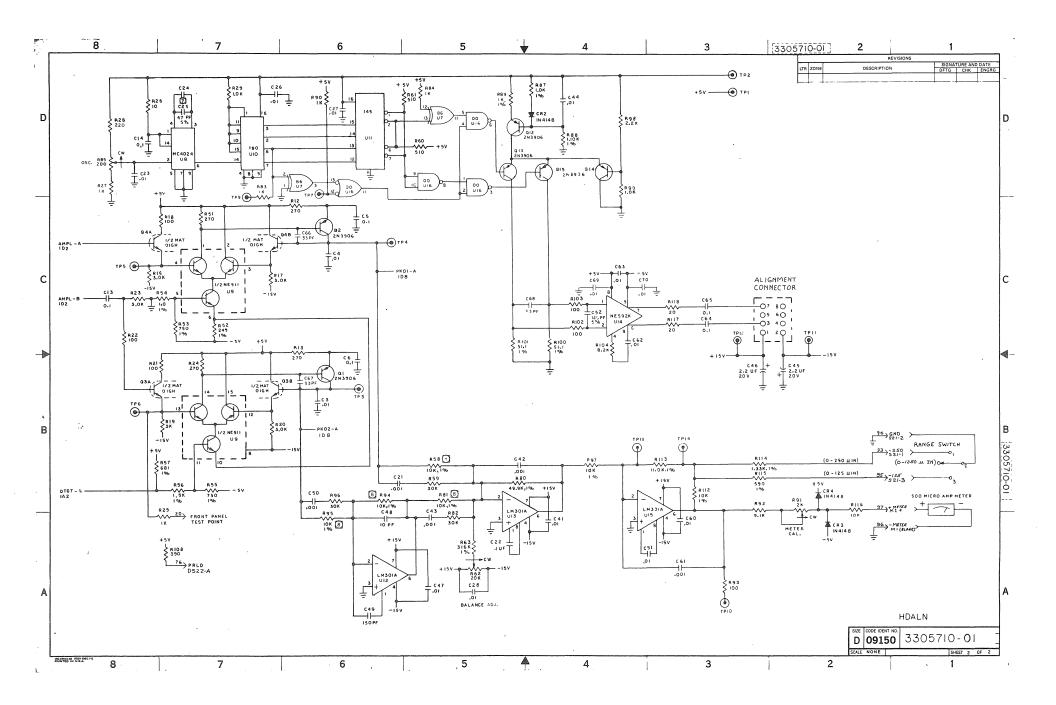
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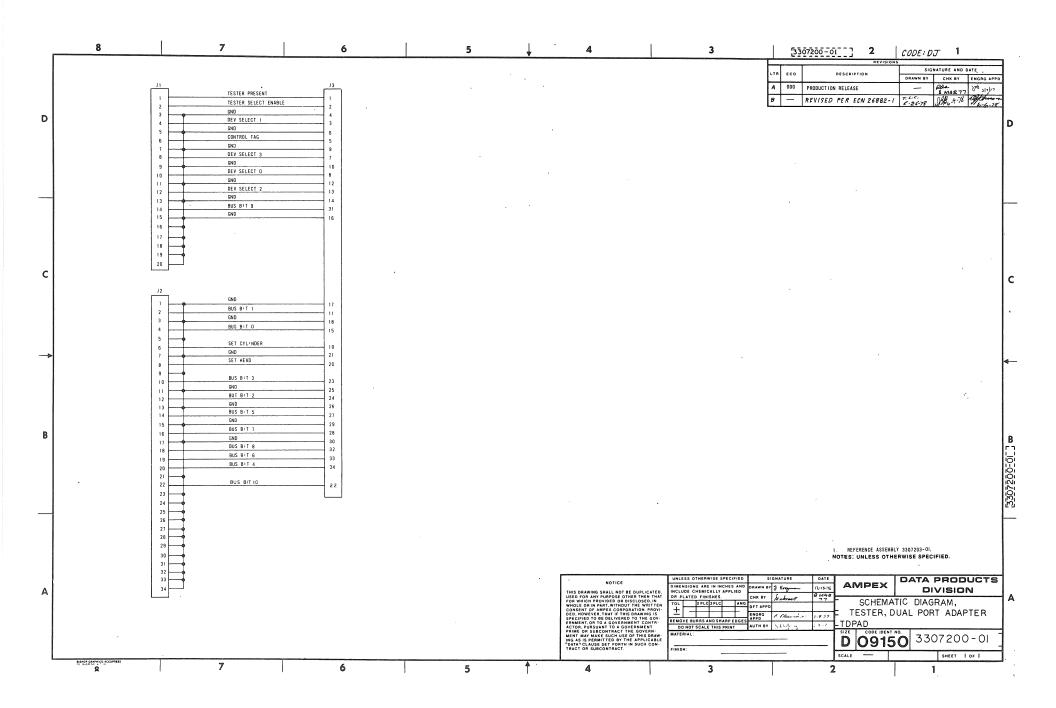


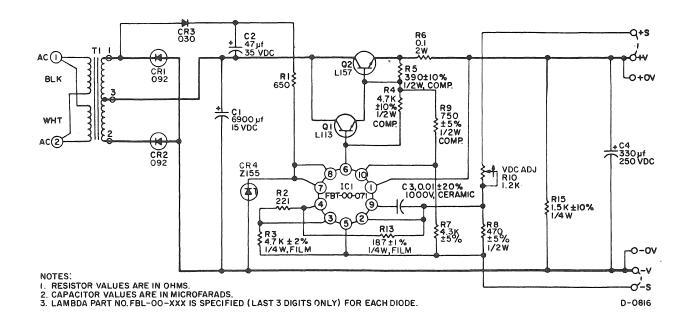


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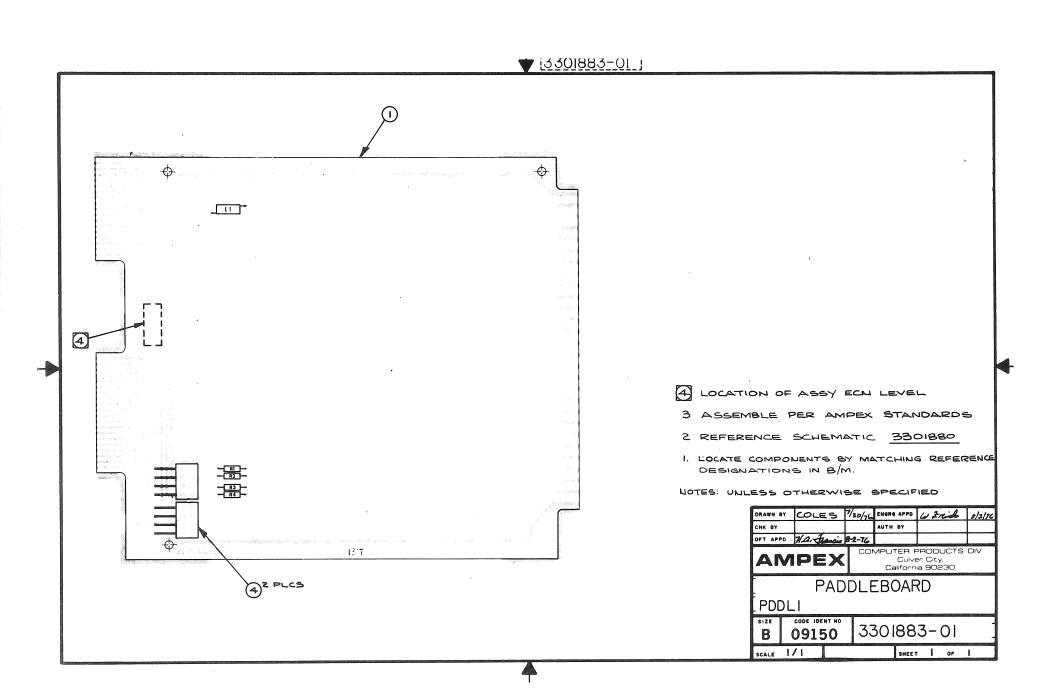


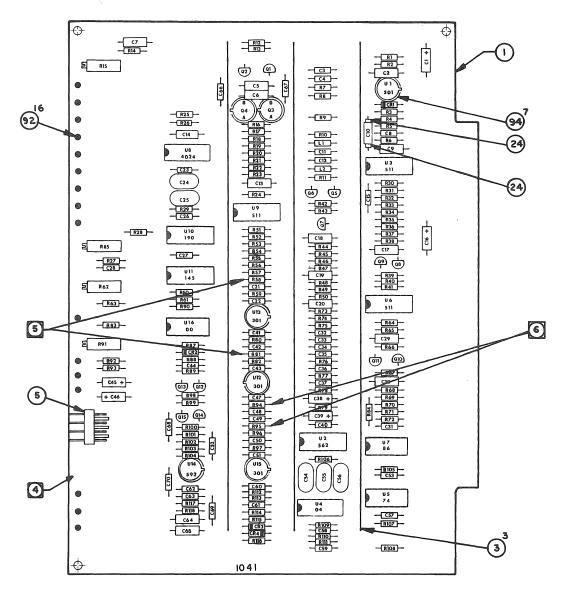




+5 V POWER SUPPLY

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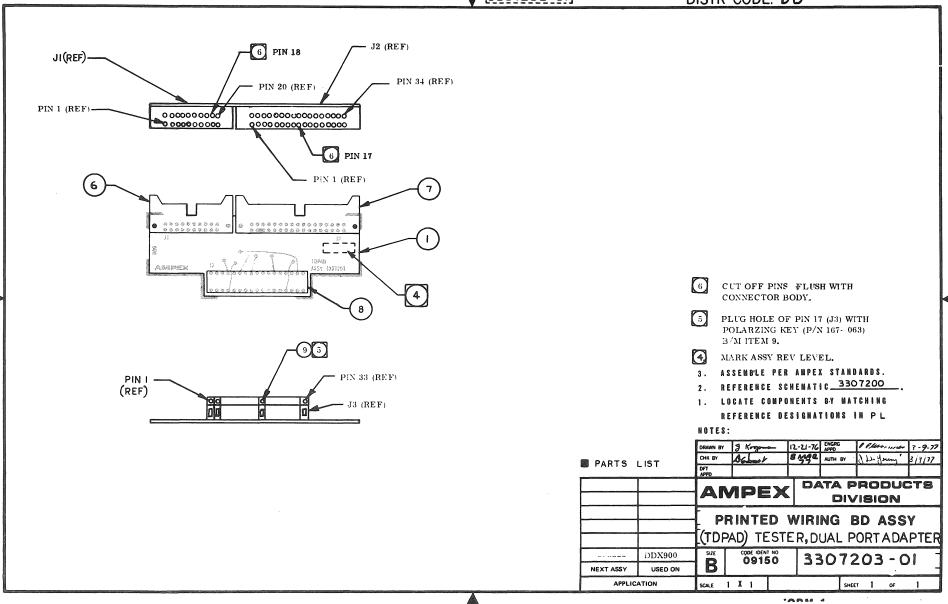


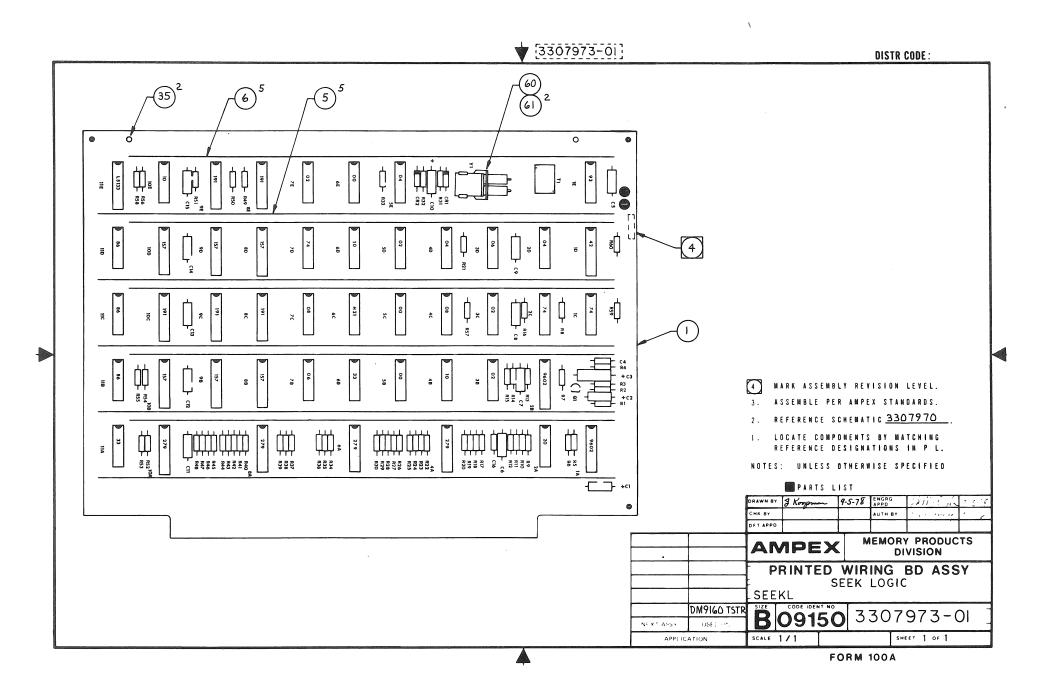


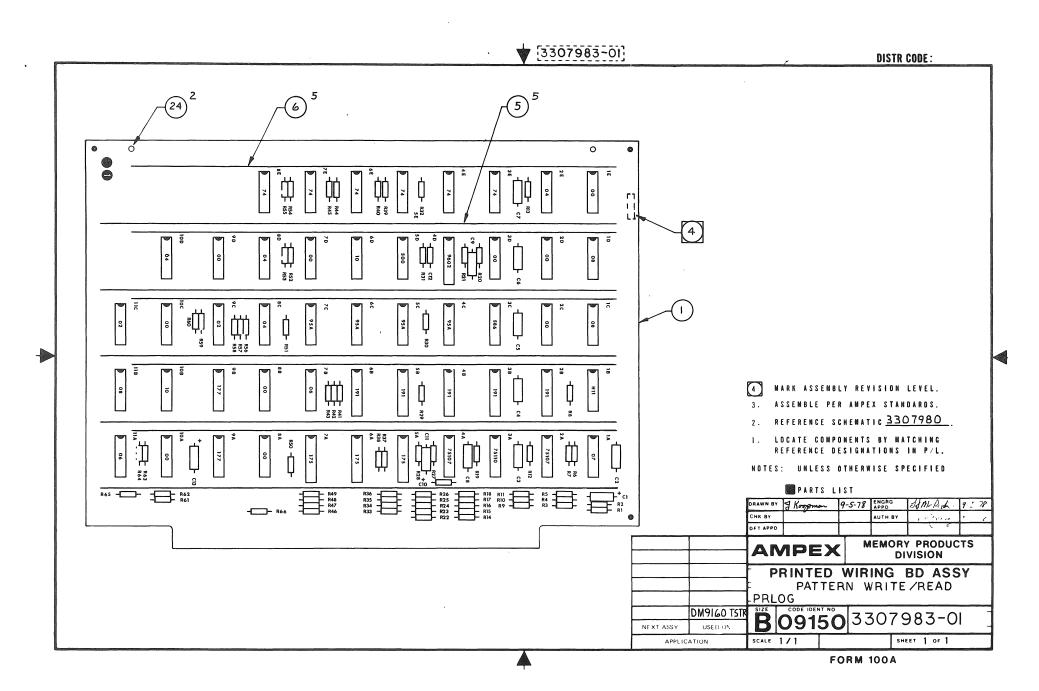
HEAD ALIGNMENT (HDALN) 3305713-01

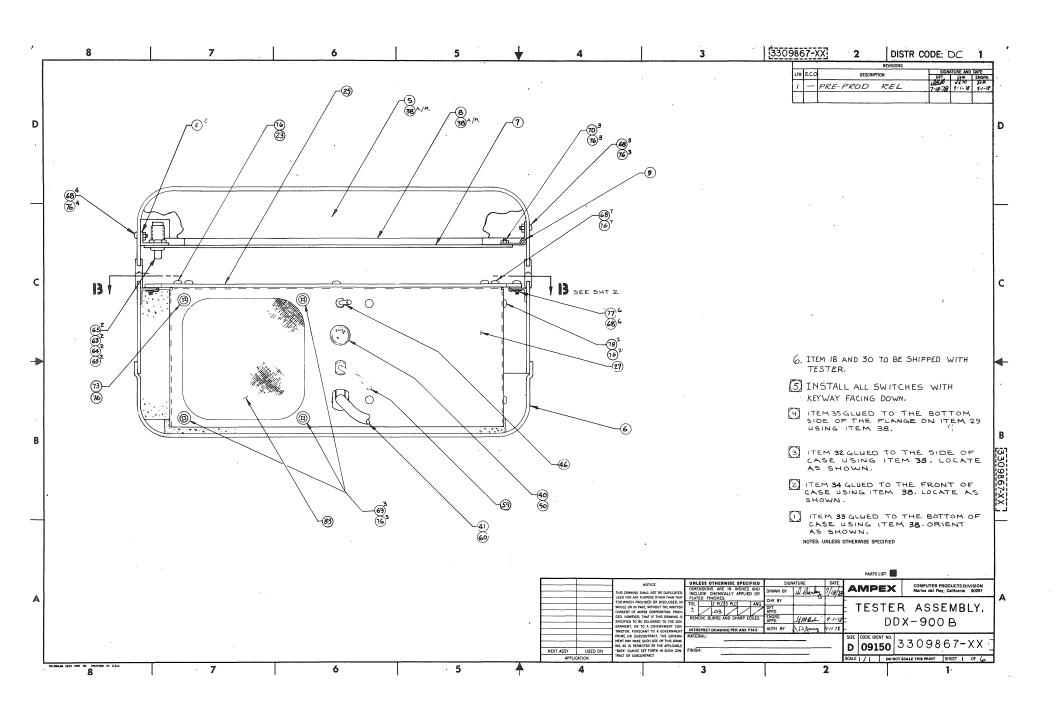
- 6 R94 & R95 MATCHED PAIR PER DWG. NO. 3301765-01.
- 5 R58 & R81-MATCHED PAIR PER DWG NO. 3301765-01.
- 4 LOCATION OF ASSY ECN LEVEL
- 3. ASSEMBLE PER AMPEX STANDARDS.
- 2. REFERENCE SCHEMATIC 3305710
- I. LOCATE COMPONENTS BY MATCHING REFERENCE DESIGNATIONS IN B/M.
  NOTES:

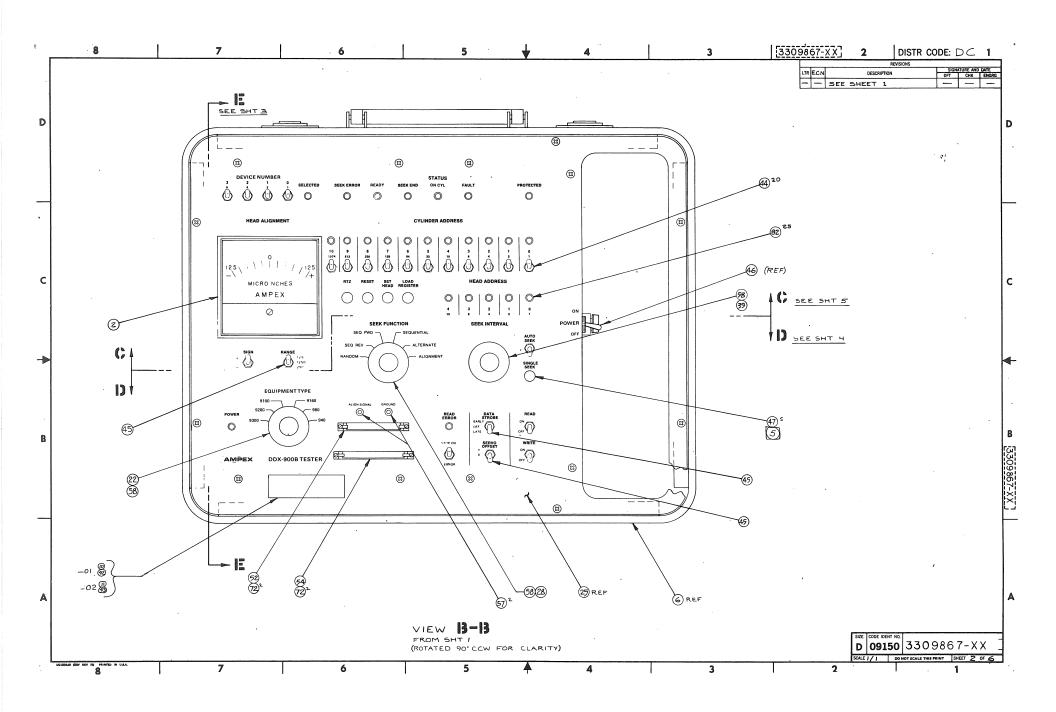
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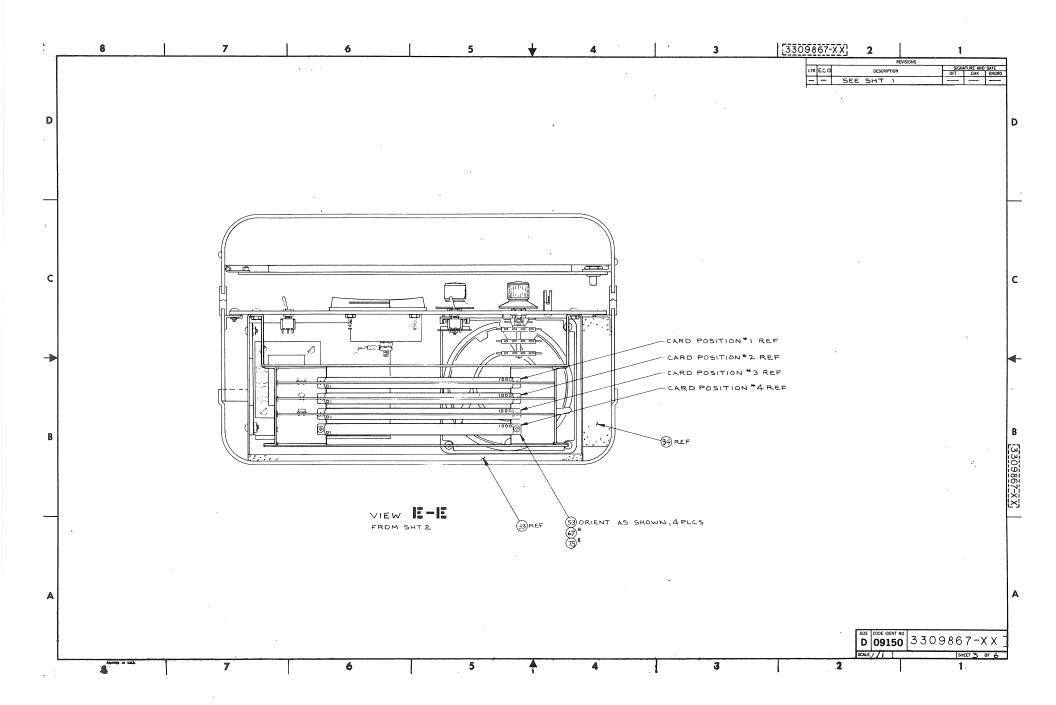


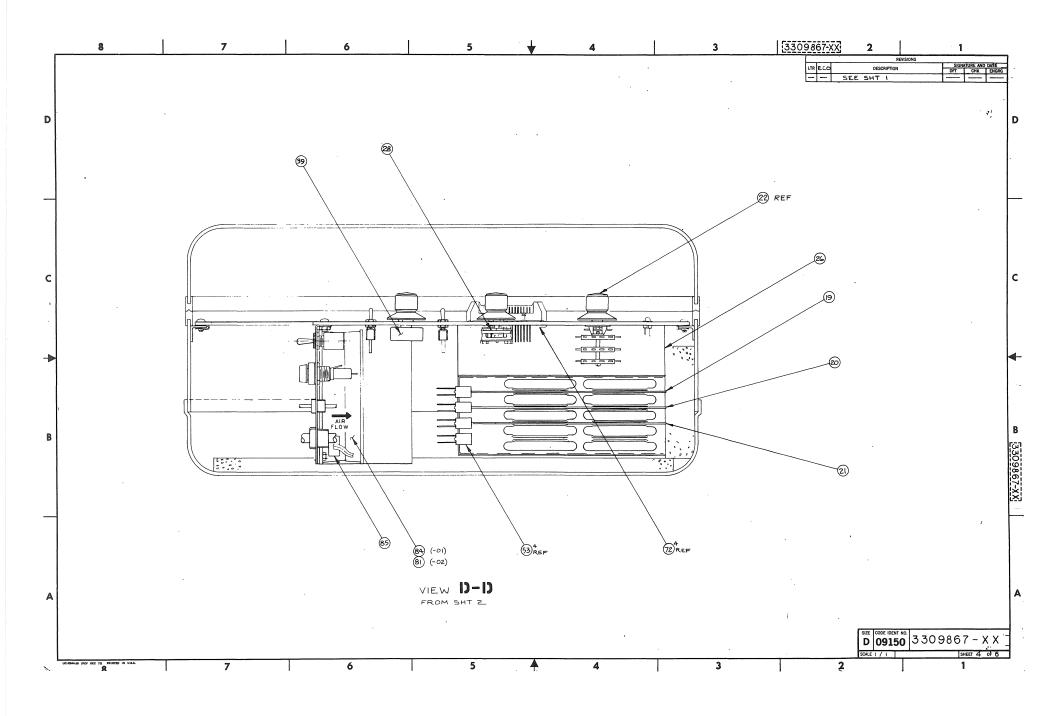


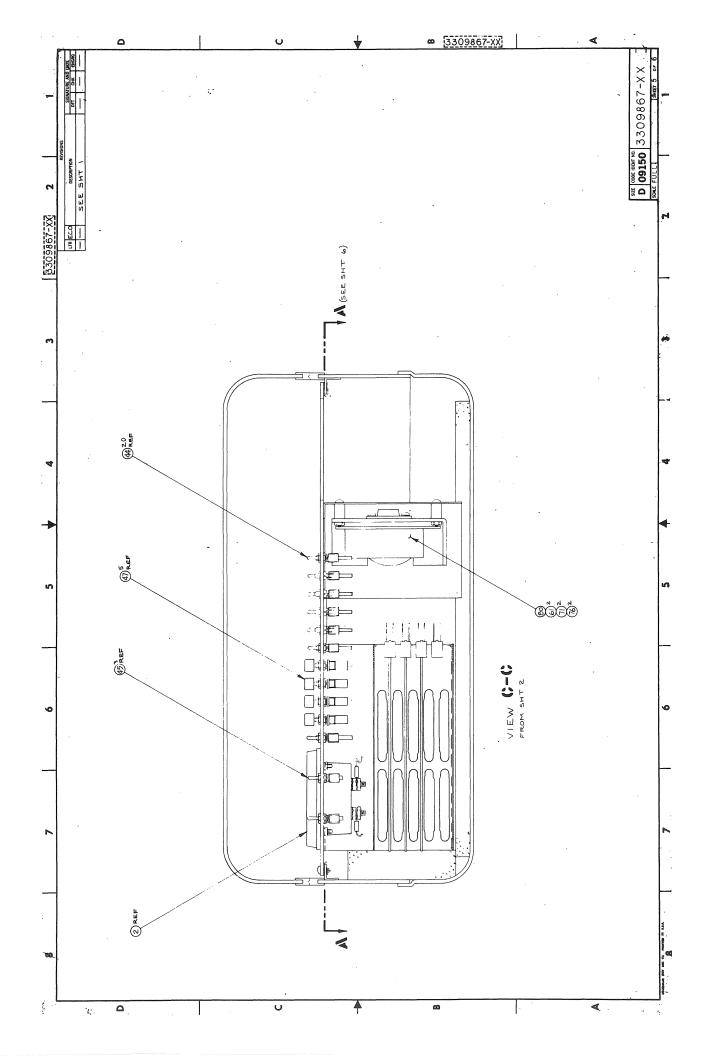


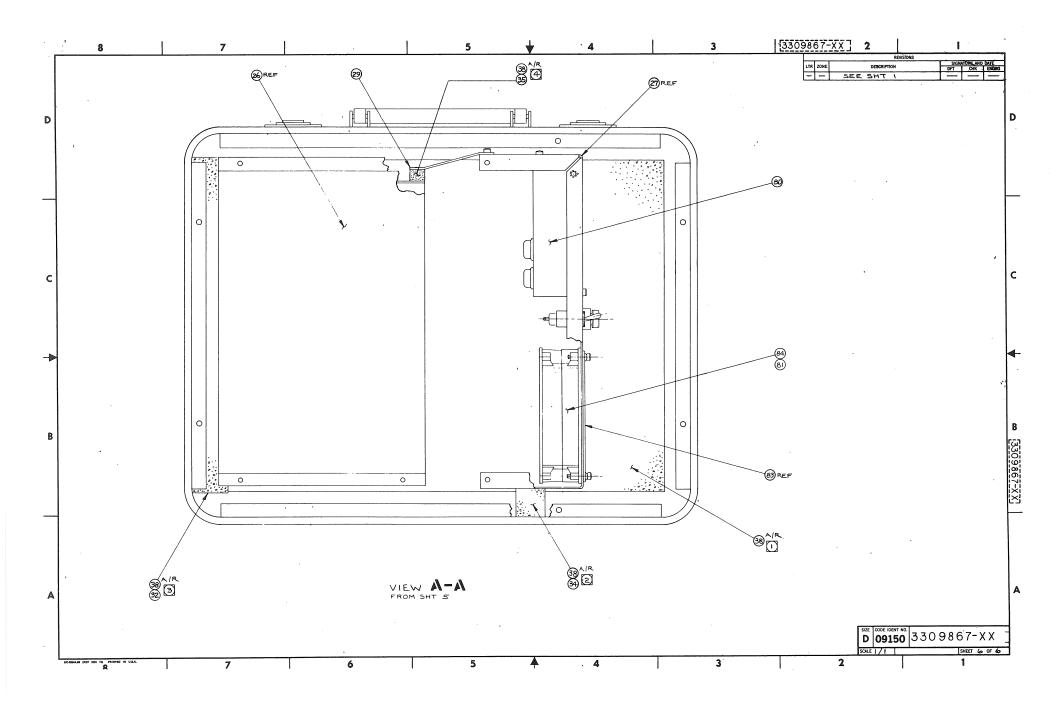












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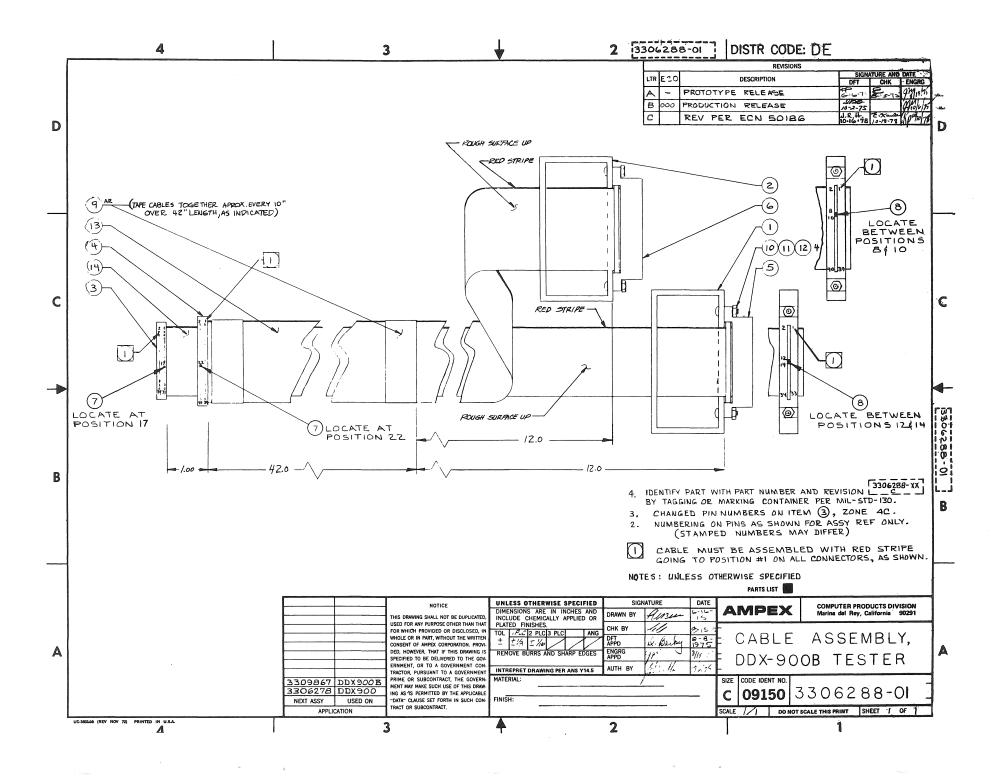
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33	С	3306417	01	PAD, FOA	M, TOP		1	1	-	-				-
34	В	3306418	01				1	1	-	-	ļ		-	<u> </u>
35	В	3306437	01		M, AIR DEFLECTOR		1	1				<u> </u>		
36	A	3306525	0.1	OPTIONS,	FOR DM-9000 SERIES		REF	REF						
37	A	3306526	0.1	OPTIONS,	FOR DM900/9160 SERIES		REF	REF					<u> </u>	
38		018-392		ADHESIVE	, EPOXY	•	<del>-</del>	A/R	<u> </u>			<u></u>		
39		058-927		RESISTOR	, VAR., 250K ±30%, 1/2W	Rl	1	1						
40		070-321		FUSE, 1.	0 AMP, 250V	Fl	1	1						
41		084-066			, 3 COND, 18 AWG		1	1						
42	C	3310309	01	PLATE, ID,	110V (ASSEMBLED IN HONG	KONG)								
43	C	3310309	02	PLATE, ID,	220 V (ASSEMBLED IN HON	G KONG)								
40		119-254		SWITCH.	TOGGLE, SPDT	S1-14,18,22,23, 26,28,30	20	20						

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52		139-655		CONNECTOR	R, HEADER, 34 PIN	J1		1	1						
53		139-824			R, CARD EDGE, 100	A1,A2,A3	, A4	4	4						
54		139-831			R, HEADER, 40 PIN	JZ		1	1						
55															
5.6		171-224		TERMINAL	LUG, RING TONGUE			2	2						
57		187-221		TERMINAL	, FEED THRU	TPI, TP2		2	2						
58		230-118		KNOB, DIA	AL	R1, S16,	S25	3	3						
59		265-025		<b>B</b> USHING,	STRAIN RELIEF			1	1						
60		265- <b>083</b>		Bushing,	STRAIN RÉLIEF			1	1						
61		280-144		SPACER		-		2	2						
62		310-112		RECEPTACE	LE, LATCH			2	2						
63		310-113		RETAINER	, LA <b>TCH</b>			2.	2						
64		310 <b>-115</b>		NUT, LAT	CH			2	2						
65		310-190		LATCH				2	2						
66															
67		473-503		SCR, 4 40	x 1/2, PNH			8	8						
68		473-497		SCR, 6-32	x 3/8,, PNH			20	20						

\* .

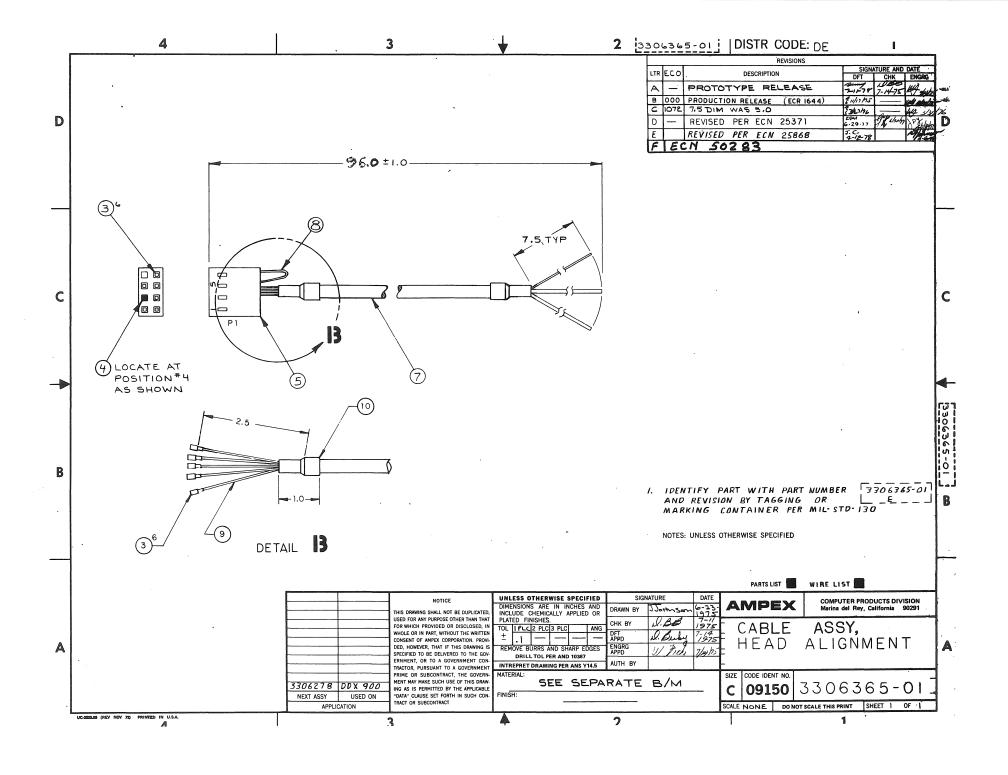
			,)

PAI	RTS	LIST	AR	<b>APEX</b>	MEMORY PRODUCTS DIVISION	CODE IDENT		P			SHEET		OF 4		REV
ITEM	DWG	PART/DRAWING NUMBER	-xx		DESCRIPTION	REFER	ENCE		QUAN	TITY R	EQUIR	ED PE	RASS	EMBLY	
69		473-534		SCR, 6-32	x 3/4, PNH			3	3	-03	-04	-05	-06	-07	-08
70		473-508			x 3/8, Flh, 82 <sup>o</sup>			3	3						
71		473-529			x 7/8, PNH			2	2					With Marie Control	
72		476-432		SCR, 4-40	x 3/8, PNH TAPPING TYPE C			4	4						
73		471-685			x 2 1/4, PNH, SST			1	1						
74															
75		498-440		NUT, 4-40	, HEX, W/XT-LK			8	8						
76		496-002		NUT, 6-32	, HEX, W/XT-LK			28	28						
77		498-507		NUT, SHT,	SPRING, #6-32			6	6						
78		473-269		SCR, 6-32	x 3/8 PNH			4	4						
79															
80		570-375		POWER SUP	PLY, 5V, ±5%	PSI		ı	1						
81		591-220		FAN, 230V	, 50 Hz	Bl		0	1						
82		581-271		DIODE, LI	GHT EMITTING	DS1-DS25		25	25						
83		591-195		SCREEN, G	JARD, FAN			1	1						
84		591-265		FAN, 115V	, 60 HZ	Bl		1	0						
85		591-230		CORD SET,	FAN			1	1						
86															
87		615-130		WIRE, SOL	ID, INS., 26/4 (YEL)			A/R	A/R						
88		615-089		WIRE, SOL	ID, INS., 30/4 (YEL)			A/R	A/R						
89		617-754		WIRE, STR	ANDED, INS., 18/2 RED			A/R	A/R						
90		617-799		WIRE, STR	ANDED, INS., 18/5 GRN.			A/R	A/R						



DIST. CODE : DE

A	MI	PE	X PRO	DATA DDUC VISIO					MATERIALS	3	DWG SIZE C	33	0628	38- <i>0</i>	1			
EC	N	APPD	DATE	ECN	AI	PPD	DATE	DRAWN: J. JOHNSON	ENGRG APPD:	•	TITLE					SHEET	1 0	F 1
A- B-0	00	19	107	+	_			DATE: 5-20-15 CHECKED: //	DATE:		CAB	LE AS	ויזפנ	(1 <b>2</b> T)	۲.			
		11	1210	5	+	$\rightarrow$		DATE: X 19-1	AUTH BY: DATE:	112/	-אממ							
								DATE: X-19-1										
ITEM		we I						DATE: J 19 J 2 11	<u> </u>	Υ				OTV	BEOD	PER AS:	· v	
NO.	SI	WG ZE	PART NUI		-х х			DESCRIPTION			REFERENCE		- 02					-07   -08
1		3	3306289		01	<b> </b>		, CONNECTOR, 40 PIN				1						
2	1	3	3306295		01	HA	NDLE	, CONNECTOR, <b>34</b> PIN				1						
3			139-666			CC	ONNEC	TOR, SOCKET, 34 PIN				1						
4			139-710			CC	ONNEC	TOR. SOCKET, 40 PIN				1						
5			139-829	)		CC	ONNEC	TOR, CARD EDGE, 34	CONTACT			1				P		
6			139-830			ĊC	ONNEC	TOR, CARD EDGE, 40	CONTACT			1						
7			167-063			KE	EY, PO	)LARIZ <b>IN</b> G				ڬ						
8	$\perp$		167-318			KE	EY, PC	DLARIZING				2						
9	$\downarrow$		225-433		ļ	TA	APE, A	DHESIVE, .75 x .007	HK, GREY VINYL	ļ		A/E	_					
10	$\perp$	<u> </u>	<del>473-503</del>		ļ	SC	REW,	<b>4-40</b> UNC X .50 LG				4						
11	$\downarrow$		<del>198-44</del> 0		ļ	IM	JT. 4-4	40 UNC W/EXT-T L/W				4	<u> </u>		·			
12	$\perp$		501-798			. WA	ASHER	, #4				4						
13			616-623			CA	BLE,	FLAT, 40 CONDUCTO	}			54"						
14			616-724			CA	ABLE,	FLAT, 34 CONDUCTOR	?			- 55"						
						<u> </u>												
	T																	
						- 1		2										
																	$\neg$	$\Box$



AN	ЛP	EX PRO	ATA DUC1	rs V		BILL OF N	MATERIA	ALS .	DWG SIZE		33(	0636	5-01			a construction	
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C107		3/3/1/6				DATE: 7-11-75	DATE: 7/	14/75	CABLE	ASSY	7. H	EAD	AL	IGNI	MEN	Т	
D E 250	(4) (4)	11-18-78		+		CHECKED: D.B.B Date: 7-11-75	DATE:				,				_		
F 502	83 1	M 17-98-18		+-		OFT APPO: D. BERKY	DATE.		4								
- 553	00 8	7 00 7 0		+	_	DATE: 7-14-75											
ITEM	DWG	PART NUME	ER	-xx		DESCRIPTION			REFERENCE	-01	[ _ 02		REED -84			-07	r_00
1	B	3306365		01	737/T 127	O ALIGN CA				REF	1	- 03	-00	-69	-00	-07	-00
	Q.	3300303		01	AA\TI'' UT	D'ALIGN CA		<del></del>		REF		-			-		
2										-	-						-
3		167-298			CONT, S	SKT, 24-20 AWG				6							
4		167-317			KEY, CO	ONN POLARIZING				1							
5		167-320			BODY, 8	B POS RECPT				1							
6		. •							,								
7		<b>616-31</b> 2			CA, 4 C	OND, 22/0/2, 5/9				8"							
8		617-727			WIRE, 2	4/0, STRD, BLK				<b>5</b>							
9		600-543			SLVG.,	.047ID. POLY, SHK				1'							
10		600-090			SLVG.,	.187 ID. POLY, SHK. BL	.K			.2							
								-									

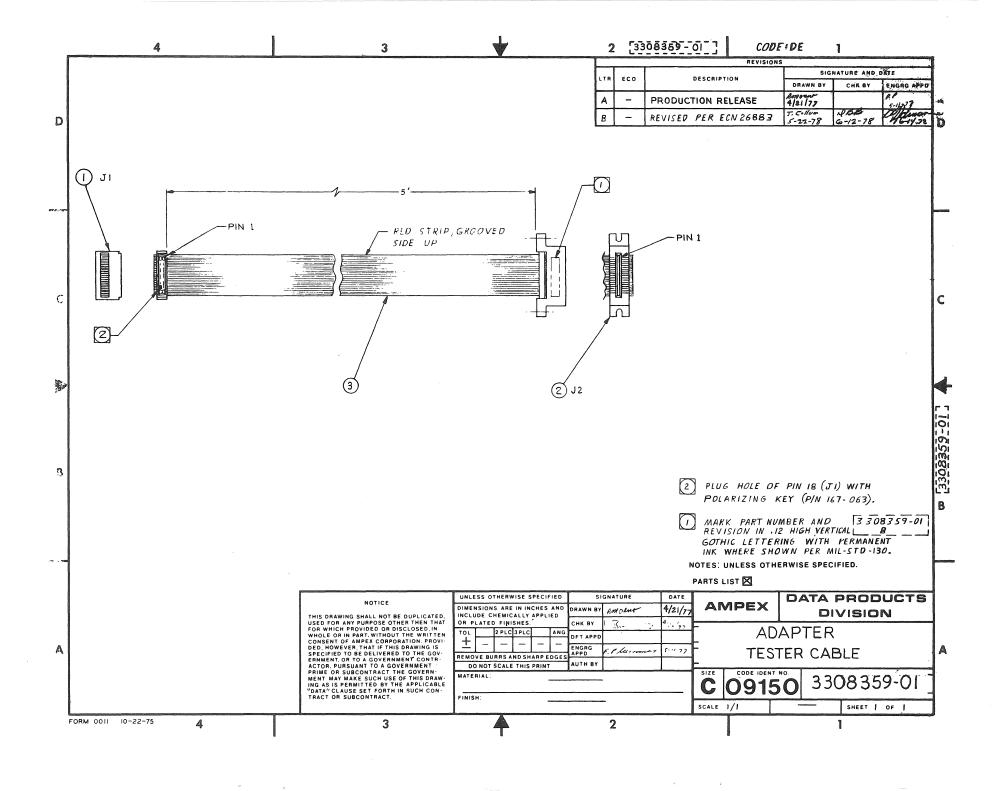
AN	/P	EX PROD	TA UCTE BION	3		BILL OF	MATERIALS	9 I	SIZE C		33(	0636	5-01				
ECN	AP	PD DATE	ECN	APPD	DATE	DRAWN: REMY	ENGRS APPD: W.F.	TITL	F				T	SHEET	1 (	)F 1	
C107	12 1	4 9/3/1/26				DATE: 7-11-75	DATE: 7/14/75							_			
D	6	1 9/3/1/6 1 1 1 1 6/30/11				CHECKED: D.B.B	AUTH BY:	'	CABLE	ASSY	, H	EAD	AL	IGN.	MEN	T	
E.258	168	11-18-78				DATE: 7-11-75	DATE:										
F 502	83	M 12-28-78				DIT APPO: D. BERKY		-1									
						DATE: 7-14-75						San Carlotte					
ITEM NO.	DWG	PART NUMBE	R -	-XX		DESCRIPTION		REFERE	NCE	-01	- 02			PER AS	87 -06	-07	(-08
1	В	3306365		01 V	V/L, HI	ALIGN CA				REF							
2								-									
3		167-298			CONT, S	KT, 24-20 AWG				6	-						
4		167-317		K	EY, CO	ONN POLARIZING				1							
5		167-320		E	BODY, 8	POS RECPT				1							
6																	
7		<b>616-31</b> 2		C	CA, 4 C	OND, 22/0/2, 5/9				8"							
8		617-727		V	VIRE, 2	4/0, STRD, BLK				- 5							
9		600-543		S	LVG.,	.047ID. POLY, SHK				1'							
10		600-090		s	LVG.,	.187 ID. POLY, SHK. B	LK			.2							
		,					-										
				·													

AMPEX CALIFORNIA

\$CO AFFO, DATE CQ AFFO, DATE F.25868

A- 154 7/14 E.25868

A- 154 7/14 E.25868 **WIRE LIST** WL 3306365-01 SHEET 1 OF 1 ENGR APPD: TITLE DATE: クリックラ CABLE ASSY, C1072 //44 D D1 HEAD ALIGNMENT DATE: BM# 3306365-01 FROM TO BM ITEM NO. REF DESIG TERMINAL REF DESIG WARE NO. GAUGE/ DESC LGTH PROCESS STA STA PROCESS REMARKS FROM WIRE то CŘIMP WRA P TW **+1**5V 1 22/2 96" P1-1 A3-81 3 2 P1-2 CRIMP WRA P A3-55 PR -15V 3 22/0 96" 3 CRIMP WRA P A3=11 7 \_ 3  $\mathbf{T}\mathbf{W}$ HEAD A 22/9 96" P1-3  $\mathbf{P}\mathbf{R}$ -4 CRIMP WRA P A3-9 HEAD B 3 22/5 96" P1-7 5 SHIELD 96" P1-5 CRIMP WRA P A3-2 GROUND 3 2" TOGETHER CRIMP P1-6 GROUND 3 6 24/0 P1-5 8



PA	RT	S LIST /	Ar	NPI	EX			401 BROAD REDWOOD		ASSY DWG SIZE	PL	_ 3	3 0	8 3	5 9	- 0	1	REV B
		REVISIONS	S			DIVISION			4063	C					1			
LTR		DESCRIPTION			DATE	SIGNATURES	DATE	CODE IDENT	CODE	DENT	CO	NTRAC	CT NU	MBER	N	EXT A	SSEMB	ILY
		DUCTION RELEA	\SE	KI.	5-11 27	DRAWN R. Moreno	421/77	09150		39					<u></u>			
B	REV	PER ECN 26883		Dhi.	C 14 3	CHECKED		DRAWING TI	TLE									
						ENGRG halfalling	5-1117		ΑĐ	АРТ	ER T	EST E	R CA	BLE				
-		***				ENGRG	-											
	· ·	·				MANAGER	<u> </u>	<u> </u>				-				- 100		
NO NO	DWG SIZE	PART / DRAWING NUMBER	- x x			DESCRIPTION		REFER	RENCE		- 01	- 02			ED PE -05			
1		139-723		CON	N, 20 1	POS		J1			1							
2		140-107		CON	N, 20 1	POS, CARD EDGE		J2			1							
3		616-829		CON	N, 20	PIN FL CABLE					51							
4		167-063		KEY	, POL	ARIZING					1							
6		3308359	01	WIR	E LIST						REF					·		
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	1		SUNNYVALE CALIFORNIA		T		MID	E LIST		WI	3308359-0	_		
1/0	APPD	DATE	ECO APPO	DATE	DRAWN: R.			ENGR APPD: A.	lamon	TITLE		SHEET	l OF	1
A-PRO RE	16	5-11-77			DATE: 4/			DATE 5-11			ADAPTER TESTER CABLE	•		-
B <b>26</b> 88	MI	6-14-78			CHECKED:			PROJ ENGR:			LESIER CABLE			
	WIRE		<del></del>		DATE:		γ	DATE:		L	BM #	<del></del>	A ITEM	NO.
WIRE	GA'IGE/	LGTH	PEF DESIG	FROM	PROCESS	STA	STA	PROCESS	REF D	ESIG	REMARKS	FROM	T	$\overline{}$
NO.	DUSC		TERMINAL				J.,		TERM	INAL				+
1	28/8	5	J1-1	c	RIMP	-		CRIMP	J2-1			1	3	2
2			JI-2		-1	ļ			J2-2			<u> </u>	-1-	H
3	-		J1-3						J2-3				$\vdash$	₩-
4	-		J1-4			<u> </u>			J2-4				Н	₩.
5	-		J1-5			<u> </u>			J2-5				$\sqcup$	11
6	_	-++	J1-6			<u> </u>			J2-6			$-\!\!+\!\!\!+\!\!\!-$	-	11-
7	_	-	J1-7		_	L			J2-7			-H	Н.	11
8	-	-	J1-8		_	ļ	L		J2-8				Ц.	11-
9			J1-9				<u> </u>		J2-9				_	11
10			J1-10			ļ			J2-10				1	Ц.
11	_ _	$-\!\!+\!\!\!\!+\!\!\!\!\!-$	J1-11			-	<u> </u>		J2-11				1	$\sqcup$
12		$\perp \perp \perp$	J1-12						J2-12			_	Ц_	$\sqcup$
13			J1-13		_		ļ		J2-13				-	₩.
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l		44	14/14/2				DATE:			DATE:			1	DDX 900					-
ŀ	WIRE	WIRE GAUGE/		RE	F DESIG	FROM		7		T	TO	REF D	ESIG	BM # 3306278-XX	F			NO.	_
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ŀ	1 2	26/4			2-1 2-2	<b>'</b>	VRA P	+	-	WI	RA P	A3-5	,	-15 VOLTS	1	_	87	-	
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ł	4	+	-		2-4		+	+				J2-6		GND	Н	Н	+	+	
ŀ	5	+	+	<b>├</b>	2-5	-	+	<b>†</b>				A2-25	,	-5 VOLTS	Н	Н	+	+	_
	€	$\neg$			2-6		1	†				A1-1		GND	Н	H	$\dagger$	$\dagger\dagger$	
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	э			J2	:-9							J2-15		GND	П		T	$\prod$	
I	10			J2	-10							75-8		GND			I	$\coprod$	
1	11			J2	-11							A2-1	5	SERVO CLK -N	Ц		$\perp$		
L	12			J2	-12							J2-10	,	GND	Ц		$\perp$	$\perp \! \! \! \! \! \! \! \! \! \! \perp$	
1	13		<u> </u>		-13			4				A2-17		SERVO CLK -P	Ц		$\perp$	$\coprod$	_
-	14		-	<del>                                     </del>	-14	-	+					J2-12		GND	Ц	$\perp$	4	$\coprod$	_
-	15		-	<del> </del>	-15	+	+					J2-21		GND	Н	$\dashv$	+	+	_
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ŀ	17	+	+		-17	_	+	+-+				A2-28		READ CLK -P	Н	$\dashv$	+	+	-
ł	18				-18	-	+	+				J2-2		GND READ CLK -11	Н	$\dashv$	+	+	-
ŀ	20	_	+		-19 -20		+	+				A2-26		GND	Н	+	+	++	-
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t	22	$\dashv$			-22		1	$\dagger$						KEY	П	+	$\dagger$	#	7
t	22	$\top$			-23		1					A 2-23		READ DATA -N		1	$\dagger$	$\dagger \dagger$	٦
T	24	$\top$		J2-	-24							A2-97		INDEX -L			T	$\top$	٦
I	25			J2-	-25							A 2-25		READ DATA -P				$\Box$	
	2€			J2-	-26					-		A2-12		SEEK END			I	$\prod$	
L	27			J2-	-27							J2-33		GND	Ц	i_	$\perp$	$\perp \! \! \! \! \! \! \! \! \! \! \perp$	
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L	29			J2-	-29	_	-	$\perp$				A2-18		WRT CLK -P	$\sqcup$	ì	1	4	4
F	30			J2-	-30	_						A1-12		ON CYL -L	Н	— <u>i</u> -	+	+	4
H	31				-31		-	+				. A2-20		WRT CLK -N	Н	+	+	+	4
F	32	-	+		-32	+	+	+-+				A2-6	$\dashv$	SEEK ERROR -L	H	+	+	╁╂	-
H	33		+	J2-		-	+	+				J2-39 A2-8	-+	GND FAULT -L	Н	+	+	++	-
f	35	$\dashv$	+	J2-		-	+	+				A2-21		WRT DATA -P	H	+	+	+	1
F	36		+	J2-		_	1	† †	$\dashv$	1		A3-85		READY -L	$\dagger$	Ť	+	$\dagger \dagger$	1
r	37		+	J2-			1					A2-19		WRITE DATA -N	$\parallel$	1	+	$\prod$	1
r	38			J2-								A2-10		PROTECTED -L	П	_ i	T	$\prod$	1
	39			J2-	-39		-			-		A2-2		GND	4	, [	T		
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AMPEX SUNNYVALE CALIFORNIA
CO APPD DATE ECO APPD **WIRE LIST** WL 3303828-01 ENGRAPPO: W HREAK DRAWN: REMY TITLE SHEET 1 OF 1 DATE: Y/1/75
PROJ ENGR: 8/21/2 8-11-75 DATE: CHECKED: AC & DC POWER B000 /// 13/16/20 DDX 900 1/17/16 DATE: DATE: BM # 3306278-XX BM ITEM NO. WIRE NO. GAUGE/ DESC REF DESIG TERMINAL FROM WIRE STA-STA LGTH PROCESS PROCESS REMARKS TO PWR CORD-G SOLDER P.S. C. .1 P.S. GND LUG 18/5 PWR CORD-B END LUG F1 2 41 18/6 F1-1 \_ 3 18/9 PWR CORD-W P.S. AC 2 WHITE WIRE 4 18/2 F1-2 SOLDER S27-1 SIDE LUG OF F1 \_ 89 18/2 SOLDER P.S. AC 1 89 5 827-2 EXISTING WIRE EXISTING WIRE B1-1 BLOWER AC 6 P.S. AC 1 85 BLOWER AC B1-2 P.S. AC 2 8 P.S. GND LUG TO 18/5 \_ P.S.C. SOLDER SOLDER P.S. -V 90 9 10 26/4 P.S. + V SOLDER WRA P 87 +5V A 1-4 A1-3 87 11 26/4 P.S. + V +5V 12 A2-3 87 26/4 P.S. + V +5V A3-3 13 26/4 P.S. + V SOLDER WRAP +5V 87 14 15 16 WRAP A1-2 GND 87 SOLDER 26/4 P.S. - V GND 87 17 A1-100 26/4 P.S. - V A3-1 GND 18 P.S. - V 87 26/4 A3-99 GND 19  $\mathbf{WRA}\,\mathbf{P}$ -87 26/4 P.S. - V SOLDER

CODE: DJ

<del>-</del> ,	V. H - 1	-78	CALIFORNIA				AAIN	E LIST		WL	3309875			_
rco 	APPD	DATE	ECO APPO	DATE	DRAWN S.			DATE. 17-1	VerReddin VX	TITLE		SMEET	1 0	,
	.dsm	11-2-78		<b>†</b>	CHECKED			PROJ ENGR		CONT	ROL PANEL WIRING			
50213					DATE .	. 1 1	*	DATE		L		γ		
MRE	GAUGE/	LGTH	REF DESIG	FROM	PROCESS	STA	STA	PROCESS	REF D	ESIG	BM # 3309867-XX	FROM	M ITEM	7
1	DESC		TERMINAL DC 5 A	_	SOLDER	-	<del>                                     </del>	SOLDER	DS4-			+-	37	+
2	26/4	_	DS5-A DS4-A	<del></del>	A SOLDER	<u> </u>	<del>                                     </del>	SOLDER	DS24			1	T A	+
3	T	+-	DS24-A		-F		1		DS3-			†Ť	ΤŦ	+
4		1	DS3-A		1	1	<u> </u>		DS23	-A		TT	$\dagger \dagger$	1
5			DS23-A					V	DS2-	A		$\prod$	$\Pi$	1
6			DS2-A					SOLDER	DS1-	A		$\prod$	$\prod$	
7			DS1-A					WRAP	A1-3		+5 VOLTS		П	I
8		i	DS25A					SOLDER	DS15	-A	+5 VOLTS	Ш	Ш	1
9			DS15-A	1		<u> </u>	<u> </u>	SOLDER	DS14	-A		$\perp \perp$	Ш	1
10	<u> </u>		DS14-A					<b></b>	DS13	-A		$\sqcup \downarrow$	Ш	1
11			DS13-A				ļ		DS12	-A		$\downarrow \downarrow$	$\sqcup$	4
12		-	DS12-A		·		<b> </b>		DS11	A		++	11.	4
13			DS11-A				<del> </del>		DS10			++	++	+
14			DS10-A						DS9-			++	++	+
15		+	DS9-A			-		1-1-	DS8-			++	++	+
16		+	DS8-A	-		ļ	<b> </b>	COLDER	DS7-				+	+
17	26//	+	DS7-A		SOLDER	<del> </del> -	<del>                                     </del>	SOLDER	A1-4		+5 VOLTS	1	87	+
18	26/4	+	DS6-A	<del></del>	SOLDER	<del>                                     </del>	<del>                                     </del>	WKAP	A1-4		+3 40712	╁	107	+
19	26//	_	DS20-A		SOLDER		<del>                                     </del>	SOLDER	DS19			†_	87	1
20	26/4	+	DS19-A		A		l	SOLDER	DS18			1	A	+
21 22			DS19-A				<u> </u>	· V	DS17			$\sqcap$	$\Pi$	1
23	-		DS17-A		<b>V</b>			SOLDER	DS16			1	1	1
24	26/4		DS16-A		SOLDER			WRAP	A2-3		+5 VOLTS	<u> </u>	87	
25											•			
26												L	1	1
26	26/4		DS21-A		SOLDER			SOLDER	R1-3			<u> </u>	87	4
28	26/4	_	R1-3		SOLDER		ļ	SOLDER	R1-2			ļ-	87	4
29	26/4		R1-2		SOLDER		ļ	WRAP	A2-4	·	+5 VOLTS	<u>├</u> -	87	'
30			ļ				<u> </u>		ļ			-	100	4
31	26/4		S4-3		WRAP			WRAP	S3-3			-	87	4
32	-1-	+	S3-3				<del>                                     </del>	<u> </u>	S2-3 S1-3			+1	+7	+
33		-	S2-3		<del>-  </del>	<del>                                     </del>	<del>                                     </del>	<del> </del>	S26-			++	++	+
34		-	S1-3 S26-2		-	<del> </del>	<del> </del>	<del>  </del>	S14-			++	+ +	+
35	_	+	S26-2 S14-2		_	<b>†</b>			S13-			++	$\dagger \dagger$	+
36 37	-	-	S14-2 S13-2				<del>                                     </del>		S12-			++	$\dagger\dagger$	+
38	$\top$	+	S12-2						S11-			††	11	+
39		1	S11-2				1		S10-			$\prod$	$\prod$	1
40			S10-2						S9-2	2			$\prod$	
41			S9-2						S8-2	2		П	П	
42			S8-2			ļ	ļ		S7-2	2		$\prod$	Щ	
43			S7-2		_		L		S6-2	<u>,                                      </u>		11	44	_
44		-	S6-2		<b>V</b>		<u> </u>	<b>V</b>	S5-2			1	1	_
45	26/4	-	S5-2		WRAP	<b></b>	<del> </del>	WRAP	A1-9	99	GROUND .	<del>  -</del>	87	4
46		+	<del> </del>			-			<del> </del>			+-	+	4
47		+	<del> </del>	-		<del> </del> -	<del> </del>	ļ	<del> </del>			+-	+	-
48		+-	<del> </del>			-	<del> </del>		<del> </del>			+-	+	+
50		+	<del> </del>				<del> </del>		<del> </del>			+	+	$\dashv$
		+	<del> </del>			<del> </del>	<del> </del>	<del> </del>	<del> </del>			+	+-	-
51	· .	+	<u> </u>			-	<del> </del>	<del> </del>	†			+-	+	+

Δ	MPEX SUNNIVALE WII			WIRE	LIST		WL	3309875-01	-	Harris				
ECO	APPD	DATE	ECO APPD	DATE	DRAWN			ENGR APPD:		TITLE		HEET	2 <b>O</b> F	4
				-	DATE.			DATE: PROJ ENGR:			rol panel wiring			-
	-				DATE:			DATE:		DD.N				
	WIRE	·		FROM				10	REF D	- I	BM# 3309867-XX	<del></del>	M ITEM	_
NO.	GAUGE/ DESC	LGTM	REF DESIG TERMINAL	'	PROCESS	STA	STA	PROCESS	TERM	INAL	RÉMARKS	FROM	-	
53	26/4		DS22-C	SO	LDER	L		SOLDER	S25A	C		-	87	<del> -</del> -
54	<b>A</b>		S25A-C	so	LDER	ļ		SOLDER	S25E	-C		1	1	1
55			S25B-C	so	LDER		-	SOLDER	S250	-C		₩	+	+-
56			S25C-C	SO	LDER	-		WRAP	S22-	2		$\vdash$	₩	$+\!\!\!+\!\!\!\!+$
57		-	S22-2	WB	AP		ļ		S21-			+	++	++-
58			S21-2	+	<del>-</del>				S20-			₩	++	++-
59			S20-C	-	-			_	S17-			$\vdash$	++	₩
60			S17-2	-	<del> </del>				S16-			+	₩	₩
61			S16-2		<del> </del>				S15-			H	₩	++-
62			S15-2	-					S31 -			+	+	₩
63	<del></del>	+	S31-2	-	1				S18-	2		1	+	+
-64			S18-2	-	▼		-		S19-			Y	- V	1
65	26/4		S19-2	WR	AP			WRAP	A2-9	9	GROUND		87	+
66	-	+	<del> </del>	+						_ +		+-	e	+
67	26/4	+	S30-2	WR	AP			WRAP	S29-	•		Ā	8.7	Ī
68		+	S29-2	+	<del></del>				S24-			H	-	Ŧ
69		+	S24-2	-	1			The state of the s	S23- S28-				+	+
70		+	S23-2	+	<u>V</u>				<del>†</del>		GROUND	- V	87	\V_
71	26/4	+-	S28-2	WR	RAP		$\vdash$	WRAP	A2-1	.00	GROUND	<u> </u>	107	+-
72	0 < 1 /	+		-			$\vdash$	COLDED	6254	_	-9293	-	87	+-
. 73	26/4		S25A-5	SO	LDER .		<b></b>	SOLDER	S25A A01-			A	107	Ā
74	<del>- T</del> -		S25A-6	+	<del>T</del> —			WRAP			-9293	HŦ	H	+7
75.		<del></del>	S25A-2	+	<del> </del>			WRAP	A01-		-0980	+	++	++-
76	<del></del>	+	S25A-1	+	<del> </del>			SOLDER	S25A A01-		-9140	++-	+	+
77		+	S25A-4		<del> </del>			WRAP SOLDER	S25A		-9140 -9660	+	tt	+
78		+	\$25A-3	-	<del> </del>			WRAP	A01-		-9660	+	+	++-
79 80		+	S25A-7 S2\$B-1	-	<del>                                     </del>			SOLDER	S25E		-5 HEAD	$\vdash$	+	+
	-+		S25B-2	1	<b>†</b>			SOLDER	S25E		-5 HEAD	$\vdash$	††	+
81		+	S25B-2 S25B-3		†			WRAP	A02-		-5 HEAD	H	++	+
83		+	S25C-1	+	1			SOLDER	S250		-LNCT	+	+	#
84			S25C-2	+	<del>                                     </del>			SOLDER	\$250		-LNCT	$\vdash$	11	+
85		+	S25C-3	1.	1			SOLDER	S250		-LNCT	H	1	+
86		+	S25C-6	+	<u> </u>			SOLDER	S250		-LNCT	+	-	1
87	26/4	<b>†</b>	S25C-7	SC	LDER			WRAP	A02-	33	-LNCT	-	87	-
88														
89	26/4	<b></b>	DS1-C	WR	AP			WRAP	A2-9		PROTECT L.E D.	-	87	-
90	A	1	DS2-C		A			A	A2-7		FAULT L E.D.	4	A	1
91			DS3-C						A2-1		SEEK END L.E.D.			$\prod$
92			DS4-C						A2-5		SEEK ERROR L.E.D		$\prod$	$\prod$
93			DS6-C						A2-5		BIT O LEG		$\sqcap$	$\prod$
94	1		DS7-C						A2-5		BIT 1 LED			$\prod$
95			DS8-C						A2-6		BIT 2 LED			
96			DS9-C						A2-5	1	BIT 3 LED		$\prod$	$\prod$
97			DS10-C						A2 - 3	5	BIT 4 LED		Ш	Ш
98			DS11-C						A2-3	8	BIT 5 LED	-	Щ	Ш
99			DS12-C						A2-4	2	BIT 6 LED			
100			DS13-C						A2-4	.0	BIT 7 LLD		Ш	$\coprod$
101			DS14-C			]			A2-3	7	BIT 8 LED			
102		<u> </u>	DS15-C						A2-3	9	BIT 9-LED	$\perp$	Ш	$\coprod$
103			S5-1		<b>Y</b>			<b>y</b>	A1-5	3	SB00+	<u> </u>	V	₩
104	26/4		S5-3	WRA	AP			WRAP	A1-5	2	SB00-	_	87	-

CODE: DJ

	SUNNYVALE CALIFORNIA							WIRE	LIST		WL	330987	5 - 01		
ECO	APPD	. A CAUFORNIA					2010/6	ENGR APPD:	W. Rida	TITLE		SHEET	1 '	OF	
.1						DATE 8	/2/78		DATE. 1-1.			DOL DAMPI GIDIN		<u> </u>	
E C R 5021	Jum	11-2-78				CHECKED	-11	:1	PROJ ENGR		DDX	ROL PANEL WIRING 9008	,		
	WIRE				FROM	DATE	- 1 1	·	DATE		L	8M# 3309867-X)		BM ITE	
nre	GAUGE/	LGTH	RE	F DESIG		PROCESS	STA	STA	PROCESS	REF C	E\$IG	BM # 3309867 -XX REMARKS	FRC	_	IRE
•	26// <sub>4</sub>	+-		5-A	+	SOLDER	<del>                                     </del>		SOLDER	DS4-			+-	3	_
-	26/4	+		4-A	+	A SOLDER	<del>                                     </del>		SOLDEK	DS24	-		+i	1°	Ĺ
-	$\neg I$	+-		24-A	+	T			<del></del>	DS3-			+1	+	F
-	_	+		3-A	+	-				DS23			+	+	$\vdash$
-	-	+	-	23-A	+	_	1-			DS2-			+	+	-
-	-+	+			+-				COLDER	+			+1	+	$\vdash$
+		+		2-A	+-	-			SOLDER	DS1-		+5 VOITS	+	+	$\vdash$
<u>'</u>	<del>- </del> -	+;		1-A	+	_	<del>                                     </del>		WRAP	A1-3		+5 VOLTS	$\dashv$	+	
-		<del> </del>		25A	+				SOLDER	DS15		+5 VOLTS	+-1	+	-
-		+	·	15-A	<del> </del>		<del>                                     </del>		SOLDER	DS14			$\dashv$	+	$\vdash$
		+		14-A	+	-				DS13			-+-	+	-
1	-	+		13-A	+		$\vdash$			DS12			+	+	-
2	$\dashv$	+		12-A	+	+-	$\vdash \vdash \vdash$			DS11	1		+	+	-
13		<del> </del> -		11-A	+		$\vdash$			DS10			++	+	
14		+		10-A	+	-	<del>  </del>			DS9-			$\dashv$	+	_
15		+		9-A	+-		$\vdash$			DS8-				+1	_
16	-	+		8-A	+	-	+		COLDED	DS7-			+1	+1	,
17		+		7-A	+				SOLDER	DS6-		15 HOLES		+	<u>_</u>
L8	26/4	-	DS	6-A	+	SOLDER	<del>  .  </del>		WRAP	A1-4		+5 VOLTS	+-	87	/
19		+			+		+	$\vdash$		+			+-	+-	_
20	26/4	+	1	20-A	+	SOLDER			SOLDER	DS19			Ā	S	7
21	-1-	-	l	19-A	+	1		L	- I	DS18	1		+1	+1	5
22				18-A	+				V	DS17	T		+	+1	7
23		+		17-A	+				SOLDER	DS16		LE VOLTE		-	_
24	26/4		DS	16-A	+	SOLDER	├		WRAP	A2-3	·	+5 VOLTS	+-	8	/
2.5		-			+					+			+	+	
26		+			+					+		· · · · · · · · · · · · · · · · · · ·	+-	+-	_
26	26/4			21-A		SOLDER	<del>  </del>		SOLDER	R1-3			+-	8	
28	26/4	-	1	3		SOLDER			SOLDER	R1-2		. F. 1101 FF2	+-	8	
29	26/4	+	Rl	-2	+	SOLDER			WRAP	A2-4	· —	+5 VOLTS	+-	8	/
30	2611				+	.ID A D	$\vdash \vdash \vdash$		LIDAD	62.5	<del></del>		+-	0	7
31	26/4	-		-3	+	√RAP Å			WRAP	S3-3			<u> </u>	8	
32		+		3-3	+	<del>-</del>		-,-	<del>- </del>	S2-3			+-1	+1	•
33		-		2-3	+	+	<del>                                     </del>			S1-3			$\dashv$	+	
34				3	+	+				S26-			$\dashv$	+	
35				26-2	+					S14-				+	-
36		+		.4-2	+		$\vdash$			S13-			+	+	-
37		+		.3-2	+					S12-			$\dashv$	╁┤	4
38		+		2-2	+	+	$\vdash$			S11-			+	+	-
39		+		1-2	+	-				S10-			$\dashv$	+	_
40		+		.0-2	+	-	<del>  </del>			S9-2			$\dashv$	+	4
41		-		1-2	+					S8-2	<del></del>		-+-}	+	-
12		+		1-2	+					S7-2			$\dashv \dashv$	+	$\dashv$
43		+		1-2	+		<del>  </del>			S6-2			$+ \frac{1}{2}$	+1	,
44		+		<u>5 - 2</u>	+	<b>V</b>	├			S5-2				+-	
15	26/4	+	S5	i-2	+-	JRAP	$\vdash$		WRAP	A1-9	9	GROUND .	+-	8	4
46	<del></del>	+			+					<b>+</b>			+	+	4
47		+			+					<del> </del>			+	+	-
48		+			+					<del> </del>				+-	$\dashv$
49		+			+					-			+	+	_
50		┼			+					1			+-	+	4
51					ı			1		1	- 1		1	1	- 1

	AMPEX SUNNYVALE W				WIR	LIST		WL	3309875-01					
ECO	APPO	DATE	ECO APPO	DATE	DRAWN		popur supra rituriina	ENGR APPD:		TITLE	_	HEET	2 <b>OF</b>	4
<u> </u>	+				DATE. CHECKED:			DATE: PROJ ENGR:			TROL PANEL WIRING			
					DATE:			DATE:						
Wilte	WIRE GAUGE/	LGTH	REF DESIG	FROM	PROCESS	STA	STA	PROCESS	REF DE	SIG	BM# 3309867-XX REMARKS	FROM	WIRE	_
MO. 53	26/4	1	DS22-C	sc	LDER			SOLDER	S25A			-	87	†-
54	<b>A</b>	<b>†</b>	S25A-C	-	DLDER			SOLDER	S25B	-C		4	A	1
55			S25B-C	sc	LDER			SOLDER.	S25C	-C				$\prod$
56			S25C-C	sic	LDER			WRAP	S22-	2		Ш		$\coprod$
57		<u> </u>	S22-2	WB	RAP		Ŀ		S21-	2		11	11	11
58		ļ.,	S21-2	1	<b>A</b>				S20-			$\sqcup$	#	4
59		ļ	S20-C		-			_	S17-			$\vdash$	₩	#
60		<del> </del>	S17-2	┼	-				S16-			$\vdash$	+	₩
61			S16-2						S15-			H	╁┼	₩
62		+	\$15-2	+	-				S31-			+	++	╁
63		<del>-</del>	S31-2	+	1			-	S18-			+	+	+
64		+	S18-2	+	<b>V</b>			V V	S19-	1	CROIND	V	87	+*
65	26/4	+	S19-2	- WE	RAP			WRAP	A2-9	7	GROUND	<u> </u>	101	+
66 67	2611	+	S30-2	LIE	RAP			WRAP	S29-	2		-	87	1_
68	26/4	†	S29-2	WE	A			WRAI	S24-			1	A	<b>A</b>
69		1	S24-2	<del>                                     </del>					S23-			П	•	$\prod$
70	<b>V</b>	1	S23-2		<b>V</b>			V	S28-				V	V
71	26/4		S28-2	WF	RAP			WRAP	A2-1	00	GROUND	_	87	Ι-
72														
73	26/4		S25A-5	sc	LDER			SOLDER	S25A	-6	-9293	-	87	-
74	<b>A</b>	<u> </u>	S25A-6		<b>A</b> ·			WRAP	A01-	26	-9293	1	1	1
75.		ļ	S25A-2		<b></b>			WRAP	A01-	24	-0980	H	11	1
76		↓	S25A-1	-	1			SOLDER	S25A		-9140	H-	$\vdash \vdash$	1
77			S25A-4	+	1			WRAP	A01-		-9140	H-	₩	+
78		+	S25A-3	-	<del> </del>			SOLDER	S25A		-9660	$\vdash$	₩	+
79		+	S25A-7	+	1			WRAP	A01-		-9660	$\vdash$	+	+
80		+	S2\$B-1	+	-			SOLDER	S25B S25B		-5 HEAD	$\vdash$	╁┼	+
81		+	S25B-2	+				SOLDER WRAP	A02-		-5 HEAD	+	++	+
82		+	S25B-3 S25C-1	+	1			SOLDER	S25C		-LNCT	+	$\dagger \dagger$	╁┼╌
84		1	S25C-2					SOLDER	S25C		-LNCT	+	$\dagger \dagger$	$\dagger \dagger$
85			S25C-3					SOLDER	S25C	-6	-LNCT	1	T	$\top$
86	<b>V</b>		S25C-6	1	<b>V</b>			SOLDER	S25C		-LNCT	-	V	V
87	26/4		S25C-7	sc	DLDER			WRAP	A02-	33	-LNCT	-	87	-
88														
89	26/4		DS1-C	WR	RAP			WRAP	A2-9		PROTECT L.E D.	-	87	-
90	-		DS2-C	ļ					A2-7		FAULT L E.D.	4	1	<b>A</b>
91		-	DS3-C	-	1				A2-1		SEEK END L.E.D.	$\perp$	$\vdash$	#
92		+	DS4-C	<del> </del>					A2-5		SEEK ERROR L.E.D	-	-	+-
93	$\rightarrow$	+	DS6-C		+				A2-5		BIT O LEEL	+		+
94	-	+	DS7-C	-	+				A2-5	1	BIT 1 LED	+	++-	+
95		+	DS8-C	+	+				A2-6	1	BIT 2 LED	+	-	+
96 97		+-+	DS9-C DS10-C	+	1			-	A2-5 A2-3		BIT 3 LED BIT 4 LED	+	++	++
98		1	DS10-C DS11-C	†	1				A2-3		BIT 5 LED	+	$\vdash$	H
99			DS12-C	<u> </u>					A2-4	<del></del>	BIT 6 LED	$\top$		$\sqcap$
00			DS13-C	1		-			A2-4		BIT 7 LUD	$\top$		$\sqcap$
01			DS14-C						A2-3		BIT 8 LED	$\top$		$\prod$
02			DS15-C						A2-3		BIT 9-LED			
103	<b>V</b>		S5-1		<b>V</b>			V	A1-5	3	SB00+	V	V	<b>V</b>
L04	26/4	1 1	S5-3	WRA	AP ]	I		WRAP	A1-5	2	SB00-	-	87	-

			SUNNYVALE CALIFORNIA					RE LIST W			<b>VL</b> 3309875-01				
6CO	APPO	DATE	ECO APPD	DATE	DRAWN:			ENGR APPD		TITLE		SHEET	3 0	4	
					DATE CHECKED:			PROJ ENGR:		CONT -XGG	ROL PANEL WIRING 9^03				
	<del>  </del>			<b></b>	DATE-			DATE:		, , , ,	, , <u>,</u>				
	WIRE			FROM		7		TC		BM # 3309867 - XX		BAA ITI		NO.	
WIRE	GAUGE/ DESC	LGTH	REF DESIG TERMINAL		PROCESS	STA	STA	PROCESS	TERM		REMARKS		A Water	10	
105	26/4		S6-1		JRAP	-		WRAP	A1-5		SB01 +	1-	87	- 	
106		<del></del>	\$6-3		4	-	L		A1-4		SB01 -	1	1	1	
107			S7-1	-		-			A1-6		·SB02 +	$\dashv$	++	#	
108		-	S7-3			ļ			A1-6		SB02 -	++	+	+	
109		-	S8-1						A1-7		SB03 +	++	+	₩	
110			S8-3 S9-1	+		<del> </del>			A1-6		SB03 - SB04 +	++	╁	++	
111		+	S9-3	+-					A1-7		SB04 -	+	++	+	
113		+	S10-1	+		-			A1-7		SB05 +	+	+ +	++	
114		+	S10-3	+-	_	<del> </del>			A1-7		SB05 -	+	++	+	
115		+	S11-1	+					A1-7		SB06 +	++	++	H	
116		+	S11-3	+	+	<del> </del>			A1-7		SB06 -	++	$\dagger\dagger$	#	
117		+	S12-1						A1-8	34	SB07 +	+	$\dagger \dagger$	$\dagger \dagger$	
118		1	S12-3						A1-8	30	SB07 -	11	11	11	
119			S13-1						Al-8		SB08 +	$\Box$	П	T	
120			S13-3						A1-8		SB08 -		Ti	$\prod$	
121			S14-1						A1-8	35	SB09 +	$\Box$	$\prod$	П	
122			S14-3						A1-8	38	SB09 -		$\coprod$	П	
123			DS5-C						A2-1	13	SELECTED LED	$\perp \downarrow$	$\sqcup$	$\coprod$	
124			DS16-C		_				A2-4	19	HD LED 0	$+\!\!+\!\!\!+$	$\coprod$	4	
125			DS17-C			L			A2-4		HD LED 1	+	$\bot \! \! \! \! \! \! \! \! \! \! \! \! \! \! \! \! \! \! \!$	4	
126			DS18-C						A2-5	51	HD LED 2	$\dashv \downarrow$	11	44	
127			DS19-C			1			A2-6	53	HD LED 3	++	11	#	
128			DS20-C		<u> </u>	ļ			A2-7	73	HD LED 4	++	++	#	
129		-	DS25-C		JRAP				A2-8	I.	BIT 10 LED	++	+	++	
130		-	S15-1		SOLDER	-			A1-1		+ SH SW	+	+	++	
131		+	S15-3	-	Ť	<del>  </del>			A1-1		- SH SW	++	++	+	
132		-	S16-1	+-	+				A1-3		+ RESET - RESET	++	+	+	
133	_	+	S16-3	+	+	1			A1-2		+ RT Z	++	$\dagger \dagger$	+	
134		+	S17-1 S17-3	+	+				A1-3		- RT Z	++	+	+	
136		+	S31-1		<b>—</b>				A1-4		+ LD REG	++	$\dagger \dagger$	$\dagger \dagger$	
137	$\neg \vdash$		S31-3	<del>     </del>	SOLDER				A1-3	39	- LD REG	+	$\dagger \dagger$	+	
138		<b>†</b>	S26-1		WRAP		-		A01-	_28	SB10. <b>∔</b>	11	$\dagger \dagger$	$\forall$	
139			S26-3		WRAP				A01-		SB10 -	1	11	$\top$	
140			S18-1		WRAP				A1-3		+ AUTO				
141			S18-3	I	WRAP				A1-3	1	- AUTO	$\prod$	$\prod$	$\prod$	
142	V		S19-1		SOLDER			V	A1-1	19	+ SCSW	V	V	1	
143	26/4		S19-3	:	SOLDER	$\sqcup$		WRAP	A1-2	20	- SCŞW	<u> </u>	. 87	1-	
144			ļ	_		$\sqcup$			<b></b>				↓_	1	
145	26/4		Ri-l		SOLDER	<b> </b>		WRAP	A1-6		+ INTP	-	87	-	
146	4	+	S20-1	+	4				A1-1		- ALIGN	14	17	1	
147		+	S20-2	-	-	$\vdash$			A1-1		- ALT	+	++	₩	
148		-	S20-3	+	-	<del>                                     </del>			A1-8		- SEQ -SEQ FWD	++	++	#	
149	-	+	S20-4	-	-	$\vdash$			A1-9			+	+	+	
150		+	S20-5	+	COL DED	<del>  </del>		LID - D	A1-3		- SEQ REV	+-	87	+*	
151	26/4	+	S20-6	+	SOLDER			WRAP	A1-7	<del>'  </del>	- RAND	+-	+87	+-	
152	26 / /-	+	S21-1	+	WRAP			WRAP	A3-9	93	- 250 $\mu$ IN	+-	87	+-	
153 154	26/4 26/4	+	S21-1 S21-2	1	WRAP	$\vdash$		WRAP	A3-9		RANGE SW COM	+-	87	<del></del>	
155	26/4	+	S21-2 S21-3		WRAP			WRAP	A3-9		-125 µ IN	+-	87	+	
	20/4	+	+	+		1			+				+	+	

SUNNYVALE CALIFORNIA WL **WIRE LIST** 3309875-01 TITLE
CONTROL PANEL WIRING
DDX-9003 DATE SHEET 4 OF 4 DATE ECO APPO DATE. DATE PROJ ENGR: CHECKED DATE: DATE: WIRE BM# 3309867-XX BM ITEM NO. FROM GAUGE/ DESC REF DESIG FROM WIRE 10 PROCESS STA STA PROCESS REMARKS 157 87 26/4 S22-1 WRAP WRAP A3-91 SIGN SW 158 159 160 26/4 S23-1 WRAP WRAP A2-94 +READ 87 161 26/4 S23-3 WRAP WRAP A2-96 -READ 87 A2-85 -DLSW 87 162 26/4 S24-1 WRAP WRAP 163 26/4 S24-3 WRAP WRAP A2-87 -DESW 37 164 A2-22 ERR LITE 165 26/4 DS21-C WRAP WRAP 87 166 167 هما 169 170 WRAP A2-90 +WRITE 87 26/4 WRAP S28-1 171 -WRITE A2-92 172 S28-3 -SER-A2-75 173 S29-1 -SER+ A2-77 174 S29-3 +ERHT A2-65 175 S30-1 - 87 -ERHT A2-67 WRAP 176 26/4 330-3 WRAP 177 56 CRIMP +METER WRAP A3-97 178 26/4 MI-+ 56 CRIMP 179 26/4 MI-BLANK WRAP A3-96 -METER 180 ONCYL LED 37 181 26/4 DS23-C WRAP A3-72 WRAP 87 182 26/4 DS24-C WRAP WRAP A3-92 READY LED 87 POWER ON LED 183 26/4 DS22-A WRAP WRAP A3-76 184 S1-2 WRAP WRAP J1-8 DEV SEL 0 87 -26/4 185 87 J1-3 DEV SEL 1 186 26/4 S2-2 WRAP WRAP 87 S3-2 WRAP WRAP J1-13 DEV SEL 2 187 26/4 188 26/4 WRAP J1-7 DEV SEL 3 87 S4-2 WRAP 189 A3-20 ALIGN TP 87 WRAP 190 26/4 TP 1 SOLDER 87 SOLDER WRAP A3-100 GND TP -191 26/4 TP 2

DISTR CODE: D J

D.	AMBEX SUNNYVALE				WIRE LIST						<b>WL</b> 3309876-01					
ECO	APPD	DATE	CALIFORNIA ECO APPD	DATE	DRAWN:	S.H.		ENGR APPO 3 / 1	11.6.La	TITLE		MEET	1 07	1		
-1					DATE.	8/3/78 ≅ ⊌ ;	<u>.</u>	DATE /-/	7á°		O LOGIC CHASSIS					
	<b>├</b>				1			ł		10Fe v = 1	900B					
	WIRE			FROM	DATE	·/ - / -	<del>"</del>	DATE		Ь	BM # 3309867-XX	T -	M ITEM	NO.		
BBIN	GAUGE/ DESC	LGTH	REF DESIG TERMINAL		PROCESS	STA	STA	PROCESS	REF D	ESIG INAL	MEMARKS	FIRO	M WIRE	10		
1	26/4		J1-1	1	JRAP		Commission of the Commission o	WRAP	J1-9		SPARE	-	87	_		
2	A	1	J1-2		A			<b>A</b>	Al-5		SLLECT ENABLE		A	1		
3		1	J1-3			1					DEVICE SELECT 1	$\Box$	$\top$	T		
4		1	J1-4			<b>†</b>			J1-6	,	GND	11	77	$\dagger \dagger$		
5			J1-5						A1-4		CONTROL TAG		11	$\top$		
6			J1-6						J1-1	.0	GND .					
7			J1-7								DEVICE SELECT 3	П	$\sqcap$	$\prod$		
8			J1-8								DEVICE SELECT 0		$\prod$	П		
9			J1-9						Al-1	00	GND		$\prod$	П		
10			J1-10						Jl-1	.2	GND		$\prod$	$\prod$		
11			Jl-ll						A1-8	39	BUS 1		$\perp$			
12			J1-12						A3-9		GND	$\coprod$	$\coprod$	$\perp I$		
13			J1-13								DEVICE SELECT 2	Ц	-11	Ш		
14			J1-14						11-1	6	GND	$\sqcup$	$\coprod$	$\coprod$		
15		<u> </u>	J1-15			1	<u> </u>		A1-9	8	BUS 0	$\sqcup$	$\bot \! \! \! \! \! \! \! \! \! \! \! \! \! \! \! \! \! \! \!$	$\bot \bot$		
16			J1-16						J1-1	18	GND	$\sqcup$	11	$\downarrow \downarrow$		
17			J1-17				ļ		ļ		KEY	Ц	4	$\bot$		
18	_		J1-18	_		-	ļ		A3-9	9	GND	Ш	+	4		
19			J1-19				ļ		A1-4	+3	SET CYL	$\sqcup$	Щ.	44		
20			J1-20			-	ļ		A1-4	+9	SET HEAD	$\sqcup$	-11	4		
21			J1-21			ļ	ļ		J1-2	25	GND	$\sqcup$	+	#		
22			J1-22			<del> </del>			A1-2	22	BUS 10	$\sqcup$	44	44		
23		-	J1-23				ļ		AL-S	90	BUS 3	$\sqcup$	-+-	4		
24		-	J1-24			-	ļ		AL-9	95	BUS 2	$\sqcup$	++	+		
25			J1-25			<u> </u>			AL-2	29	GND	$\vdash$	+	+		
26		<del> </del>	J1-26			<del></del>	ļ		J1 - 3	30-	GND	$\vdash$	4+	++-		
27		-	J1-27			<del></del>			Al-6	53	BUS 5	+	++	+		
28		<del></del>	J1-28			<del></del>	ļ ——		Al-5	58	BUS 7	++	++	$+\!\!+$		
29		+	J1-29	+		+			A2-1	I	GND	H	+	+		
30		<del> </del>	J1-30			<del></del>	ļ		A3-1		GND	╁┤	++	++		
31		<del> </del> -	J1-31			+			A1-6		BUS 9	╁	++	+		
32		-	J1-32 J1-33			+			A1-5		BUS 8		,	+		
33		+	J1-34	+		+		110.4.0	<del> </del>			1	+ "			
34	26/4	+	J1-34		WRAP	<del> </del>	<b></b> -	WRAP	A1-4	+4	BUS 4	-	87	+-		
-+		+	<del> </del>	+		<del> </del>			<del> </del>			$\vdash$	+-	+		
$\dashv$	2-3-	+	<del>                                     </del>	+		+			<del> </del>			+-	+-	+		
$\rightarrow$		+	<b>†</b>	+		+	<b></b>		<u> </u>			$\vdash$	+	+-		
		+	<b>†</b>			+			<b>†</b>			$\vdash$	+	+		
_		<del> </del>	<del>                                     </del>	+		+			<b>†</b>			$\vdash$	+-	+		
		+	<u> </u>			+			<b>†</b>			1	+-	+-		
		1		$\dashv$		1			1			$\vdash$	$\dagger$	+		
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74-1-13 SUNNYVALE CALIFORNIA **WIRE LIST** WL 3310017-01 ENGRAPPO JS W. R. M. A. ECO DATE ECO APPO DATE DRAWN SHEET 1 OF 2 -- [ DATE LOGIC CHEASSIS WIRING DDX-900B PROJ ENGR: CHECKED J W 1-75 DATE. BM # 3309867-XX WIRE BM ITEM NO. GAIJGE/ DESC STA STA REMARKS τo **LGTM** PROCESS PROCESS FROM WIRE 30/4 A1-3  $\mathbf{W} \mathbf{R} \mathbf{\Lambda} \mathbf{P}$ WRAP A2-3 +5V 88 2 +5V 88 A2-3 A3-3 +5V 83 3 A2-4 A1-4 30/4 A2-4 WRAF WRAP A3-4 +5V 88 5 6 7 WRAP 88 WRAP A2-1 GND 30/4 A1-1 8 A2-1 A3-1 GND 88 88 9 A1-2 A2-2 GND 10 30/4 A2-2 WRAP WRAP A3-2 GND 88 11 12 13 \_ 88 30/4 A1-99 WRAP WRAP A2-99 GND 14 A2-99 A3-99 GND 88 A1-100 A2-100 GND 88 88 GND 16 30/4 WRAP WRAP A3-100 A2-100 17 18 A2-30 -5V 88 19 WRAP 30/4 A2-29 WRAP -5V 88 20 30/4 A2-30 WRAP A3-29 WRAP 21 -5V 88 30/4 WRAP WRAP A3-30 A3-29 22 23 88 24 30/4 A3-55 WRAP WRAP A3-56 -15V 88 A3-82 +15V 25 30/4 A3-81  $\mathbf{WRAP}$ WRAP

DISTR CODE: DJ

20	MRE	₹X	SUNNYVALE CALIFORNIA		WIRE LIST					<b>WL</b> 3309876-01					
ECO	APPO	DATE	ECO APPO	DATE		S.H.		ENGR APPO 1	)1.6.Ja	TITLE	<del></del>				
-1	+				DATE.	8/3//8 = 3/3//8	),	DATE /-/	14		O LOGIC CHASSIS		,		
					1	4 - 1 .		DATÉ							
wise	WIRE GAUGE/	Ψ	REF DESIG	FROM		7		PROCESS	ner D	£SIG	BAA # 3309867-XX	FROM WIR			
MO	DESC	LGTH	TERMINAL	-	PROCESS	STA	STA		TERM	INAL		PRO	+-	-	
1	26/4	-	J1-1	1	VRAP	+	-	WRAP	J1-9		SPARE	1	87	+-	
2		<del></del>	J1-2	<del> </del>	-	+			A1-5	7	SELECT ENABLE	+1	1	1	
3		<del> </del>	J1-3	+		+	-		<del> </del>		DEVICE SELECT 1	+-+	$\dashv \dashv$	+	
4		+	J1-4	+	-	+			J1-6		GND CONTROL TAG	+	++	+	
5		+	J1-5	+		+			J1-1		GND GND	+1	++	+-	
6		+	J1-6 J1-7	+	_	+			71-1		DEVICE SELECT 3	+	+	+	
7		+		†		†					DEVICE SELECT 0	$\dagger \dagger$	$\dagger \dagger$	+	
8		+	J1-8	<del>                                     </del>	_	†			A1-1	00	GND	$\dagger \dagger$	11	$\dagger$	
9 10		<del>                                     </del>	J1-9 J1-10		_	1			J1-1		GND	$\Box$	$\top$	$\top$	
		1	Jl-ll	1					A1-8		BUS 1	$\top$	$\top \top$	$\top$	
11			J1-12						A3-9		GND	$\Box$	$\top$	T	
13			J1-13		$\Box$						DEVICE SELECT 2		$\prod$	Ι	
14			J1-14						J1-1	6	GND		П		
15			J115						A1-9	8	BUS 0				
16			J1-16						J1-1	.8	GND	Ш	$\coprod$		
17			J1-17	-		ļ					KEY	$\sqcup$	$\bot \! \! \! \! \! \! \! \! \! \! \! \! \! \! \! \! \! \! \!$	1	
18			J1-18	1		<del> </del>			A3-9	9	GND	Ш	44	1	
19			.11-19	<u> </u>					A1-4	+3	SET CYL	$\sqcup$	$\downarrow \downarrow$	_	
20			J1-20	-					A1-4	+9	SET HEAD	$\perp$	+	+	
21		-	J1-21	<del> </del>		<del> </del>			J1-2	25	GND	$\sqcup$	+	$\perp$	
22			J1-22	<del> </del>		-			A1-2	2	BUS 10	$\sqcup$	+	+	
23		+	J1-23	+					A1-9		BUS 3	++	+	+	
24		+	J1-24	+		-			AL-9		BUS 2	++	++	+	
25			J1-25	+		+			A1-2		GND	++	+	+	
26		+	J1-26	+		+			J11-3	- 1	GND	+	++	+	
27		+	J1-27						A1-6		BUS 5	++	+ +	+	
28	_	<del> </del>	J1-28	+		+			Al-5		BUS 7	$\dagger \dagger$	++	+	
29		+	J1-29	+		+			A2-1	1	GND	H	++	$\dagger$	
30		<b> </b>	J1-30 J1-31	+		†			A3-J A1-6		GND BUS 9	††	$\dagger \dagger$	+	
31 32		<del>                                     </del>	J1-31	+	1	1			A1-5		BUS 8	$\dagger \dagger$	+†	$\dagger$	
33	4		J1-33	1	<b>V</b>			<b>*</b>	A1-4	+	BUS <b>6</b>		1	1	
34	26/4		J1-34	1	WRAP			WRAP	A1-4	¥4	BUS 4	-	1	,	
-	2074			1		1							1	$\dagger$	
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$\Box$												Γ	Ι		
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		-		<b></b>			$\sqcup$		<b>↓</b>			_	1	$\downarrow$	
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SUNNYVALE CALIFORNIA 77-1-3 **WIRE LIST** WL 3310017-01 ENGR APPO JS W. RINAS DATE: 1-1-78 PROJENGE: £CO. APPD DATE ECO APPD DATE DRAWN: TITLE SHEET 1 OF 2 -- 1 LOGIC CHEASSIS WIRING DDX-900B & W CHECKED 9-1-78 DATE. BM # 3309867-XX WIRE FROM BM ITEM NO. REF DESIG TERMINAL LGTH PROCESS STA STA PROCESS REMARKS FROM WIRE 10 30/4 WRAP A1-3 WRAP A2-3 +5V 88 +5V 88 A2-3 A3-3 3 **∧1-4** A2-4 +5V 83 4 30/4 A2-4 WRAP WRAP A3-4 +5V 88 5 6 30/4 7 WRAP WRAP A2-1 GND 88 A1-1 88 8 A2-1 A3-1 GND GND 88 A2-2 9 A1-2 88 10 30/4 A2-2 WRAP WRAP A3-2 GND 11 12 88 13 WRAP WRAP A2-99 GND 30/4 A1-99 GND 88 A3-99 14 A2-99 88 15 GND A1-100 A2-100 16 30/4 WRAP WRAP A3-100 GND 88 A2-100 17 18 WRAP WRAP A2-30 -5V 88 19 30/4 A2-29 -5V 88 20 30/4 WRAP A3-29 A2-30 WRAP 21 -5V 88 30/4 WRAP WRAP A3-30 A3-29 22 23 88 -15V 24 A3-56 30/4 A3-55 WRAP WRAP A3-82 +15V 88 WRAP 25 30/4 A3-81 WRAP

F	- <del> </del>		SUNNYVALE WIF						E LIST		منسببة الكناسيس	WI	3310017-01	WL 3310017-01					
FCO	APPD	DATE	ECO	APPD	DATE	DRAWN		-	ENGR API	D.		TITLE	3310017 01	SMEET	2 <b>o</b> r	2			
-1				ļ		DATE			DATE				LOGIC CHASSIS WIR	ING		-			
	-			<b></b>	<del> </del>	CHECKED			PROJ ENC	H.			DDX-900B			-			
-	WIRE			<u></u>	FROM	DATE:		г	DATE	TO		L	BAA #3309867-XX	B.	M ITEM	NO.			
WIRE	GAUGE/ DESC	LGTH	1	EF DESIG ERMINAL	7	PROCESS	STA	STA	PROC		REF D	ESIG INAL	REMARKS	FROM	T	10			
53	30/4	5.5"			<b>—</b>	DAD	1			A.D.			-CBUD	+	100	1			
54	30/4	2.0"	1	2-91 2-84	- W	RAP		<b> </b>	WR	NP -	A1-6		-CRED +BITS 4	TI	85	Ī			
55	$\neg \uparrow$	1.5"	1	280		Ť	1	<u> </u>			A1-1		+BITS 3	<del>                                     </del>	ΤŦ	ΙŦ			
56		2.0"		2-88		1	<b>†</b>	<b>-</b>			A1-6		+BITS 2	11	††	H			
57		1.5"	1	2-78		<b>†</b>	1	<b> </b>			A1-7	70	BITS 1	11	11	11			
58		3.5"	A	2-86	1	1					A1-4	17	BITS 0	$\top$		11			
59		5.0"	1	2-79			1				N1-1		-ALIGN	$\top$	$\top$	П			
60		1.5"	A	2-24							A1-1	L <b>4</b>	+ST HD		TT	П			
61		1.5"	A	2-27							A1-1	13	+SE ON	T	Ti	П			
62		1.5"	A	2-27							A2-1	16	+SE ON	$\Box$		П			
63		6.0"		2-93			'				A1-1		-ALT	$\prod$	$\prod$	П			
64		6.5"	A	2-95							A1-7		-RAND	$\prod$					
65		3.5"	1	2-71							A1-3		-SEEK HD	$\prod$	$\prod$				
66		5.0"	A	2-83							A1-2	21	-CYL SEŁK	$\prod$		П			
67		4.0"	A	2-72							A1-3	36	-R/W CON		$\prod$	$\prod$			
68		3.5"	A	2-98							A1-5	57	-SELE	$\prod$	$\prod$				
69		2.5"	A	2-36							A1-6	50	CYL A9	Ш	$\prod$	Ш			
70		3.0"	A	2-34		<b></b>	<u> </u>				A1-6	52	CYL A8	$\coprod$	$\coprod$	Ш			
71		1.5"	A	2-44							A1-5	54	CYL A7	$\perp \perp$					
.72		1.0"	A	2-46			L				A1-4	18	CYL A6	$\bot \bot$					
73		2.0"	. A	2-43		ļ	-				A1-6	54	CYL A5	11	$\sqcup$				
74		1.0"	A.	2-41		<b></b>					A1-4	15	CYL A4	$\bot \! \! \! \! \! \! \! \! \! \! \! \perp$	$\!$	Ш			
75		4.0"	· V	2-50		<b></b>	ļ				A1-9	) 3 ·	CYL A3	41	$\sqcup$	Ш			
76		4.0"	A	2-48		<b></b>	<b> </b>	ļ			A1-9	2	CYL A2	44	$\coprod$				
77		3.0"	1	2-64		-					A1-8		CYL Al	++	11	H			
78		3.0"	t	2-62			ļ				A1-9		CYL A0	++	#	Щ.			
79		2.0"	1	2-32		ļ	<b></b>				A1-1		+SET CYL	++-	+-	-			
80		5.0"	<del> </del>	2-69	+		<b>_</b>				A1-5		-SC07	++	+-				
81		3.0"		2-68		<b></b>					A1-9		+BUS BIT 0	++	+	$\vdash$			
82		4.0"	1	2-76							λ1-2		+BUS BIT 1	$+\!\!+$	+				
83		2.0"	<del>                                     </del>	2-74	+	<del> </del>					A1-9		+BUS BIT 2	+	++				
84		2.5"	1	2-70		<del> </del>					A1-9		+EUS BIT 3	++	+-	H			
85		1.5"	<del>                                     </del>	2-57	-						A1-4		BUS 4	$+\!\!+$	$\dashv$	H			
86		3.5"	1	2-56		+					A1-2		CYL 10	+	+	-			
87 88	-	1.0"	1	3-90 2-59		<del> </del>	<del>  </del>				A3-8		HD ALIGN GATE BUS 7	+	+				
89	30/4				1.00	RAP				N.D.	A1-5		BUS 8	V	88	-			
90	30/4	1.0	A	2-61	W)	Mr			WR.	nr.	NI-:	, ,	0 000	╁╴	08	-			
91	30/4	4.0"	A	1-12	WI	RAP	<del>                                     </del>		WR	AP	A3-6	51	ON CYL	+-	88	-			
92	30/4			1-11		RAP	$\vdash$		. WR		A2-1		SELECTED	<del>  -</del>	88				
34	30/4	1.0	<u> </u>		- W1				. WK	**	n4-1		SIBBOTES	╁	1 00				
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