

pdp11

**DMC11  
IPL synchronous line  
unit user's manual**

digital



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# CHAPTER 1 INTRODUCTION

## 1.1 SCOPE

This manual provides the information necessary to install and operate the DMC11 Line Unit. It is organized into three chapters as follows:

- Chapter 1 - Introduction
- Chapter 2 - Installation
- Chapter 3 - Register Descriptions and Programming Information.

This chapter provides a general description of the two basic variations of the DMC11 Line Unit. They are the remote unit (M8201) and the local unit (M8202).

## 1.2 DMC11 LINE UNIT GENERAL DESCRIPTION

The DMC11 Network Link consists of a synchronous line unit that is controlled by a microprocessor. The DMC11 is used to interconnect PDP-11 computers in local and remote network applications.

This manual covers four models of the line unit. They all contain circuitry to accommodate DDCMP and bit stuffing protocols. However, they are controlled by the DMC11-AD microprocessor that handles only DDCMP.

### 1.2.1 DMC11-DA and DMC11-FA Line Units (Remote)

The module designation for both these line units is M8201. It contains modem control and level conversion logic that is compatible with both EIA/CCITT V24 and CCITT V35 interfaces. The DMC11-DA is shipped with a cable that accommodates only the EIA/CCITT V24 interface. This line unit has a maximum speed of 19.2K bps. The DMC11-FA is shipped with a cable that accommodates only the CCITT V35 interface and has a maximum speed of 56K bps.

### 1.2.2 DMC11-MA and DMC11-MD Line Units (Local)

Both of these line units have built-in modems. The module designation for the DMC11-MA option is M8202-YA. It operates at a speed of 1M bps over coaxial cable up to a maximum distance of 6000 feet. The module designation for the DMC11-MD option is M8202-YB. It operates at a speed of 56K bps over coaxial cable up to a maximum distance of 18,000 feet. The coaxial cable is not included with either option.

### 1.3 DMC11 LINE UNIT SPECIFICATIONS DMC11-MA and DMC11-MD Line Units (Local)

Operating Mode	Half-duplex (single cable) Full-duplex (two cables)
Data Format	Synchronous serial by bit, least significant bit (LSB) first
Character Size	8 bits
Block Check	16-bit polynomials: CRC-16 and modified CRC-CCITT
Data Rate	1,000,000 bps (DMC11-MA) 56,000 bps (DMC11-MD)
Maximum Distance	6,000 feet (DMC11-MA) 18,000 feet (DMC11-MD)
Modulation	Diphase (double frequency) NRZ
Transmitter Timing	RC oscillator, trimmable $\pm 5\%$
Receiver Timing	From received signal
Line Interface	Transformer coupled
Common Mode Rejection	500 to 1
Transmitter Signal	4 volts P-P (min.)
Receiver Signal	150 mV (min.) P-P
Cable Type	Belden 8232 or equivalent (not supplied)
Connector Type	AMP 20606X series
Mounting Space	One hex SPC slot (DD11B, C, or D), cutout permits use in end slots of backplane as well, provided the Unibus in/out slots contain low height ( $\leq 2.5$ in.) modules like the M930.
Power Consumption	3.0 A at +5 V 0.046 A at -15 V 0.018 A at +15 V

### DMC11-DA and DMC11-FA Line Units (Remote)

Operating Mode	Full- or half-duplex
Communications Channel	Private wire or switched
Data Format	Synchronous, serial by bit, LSB first
Character Size	8 bits

<b>Block Check</b>	16-bit polynomials: CRC-16 and modified CRC-CCITT
<b>Data Rate</b>	Up to 19,200 bps (DMC11-DA) Up to 56,000 bps (DMC11-FA)
<b>Interface</b>	RS232C or CCITT V24 compatible (DMC11-DA), CCITT V35 compatible (DMC11-FA)
<b>Modems</b>	Bell 208, 209 or equivalent (DMC11-DA)
<b>Signals Supported</b>	BA transmit data DB serial clock transmit (SCT) BB receive data DD serial clock receive (SCR) CC data set ready CD data terminal ready CA request to send CB clear to send CE ring
<b>Cable</b>	25 foot, with EIA connector supplied
<b>Mounting Space</b>	One hex SPC slot (DD11B, C, or D), cutout permits use in end slots of backplane as well, provided the Unibus in/out height ( $\leq$ 2.5 in.) modules like the M930
<b>Power Consumption</b>	3.2 A at +5 V 0.31 A at -15 V 0.03 A at +15 V

## **1.4 GENERAL DESCRIPTION**

### **1.4.1 Introduction**

This section provides a general description of the M8201 and M8202 Line Units.

The DMC11 Line Units (M8201 and M8202) perform the standard functions associated with a synchronous communications device. They are:

- Parallel to serial data conversion
- Serial to parallel data conversion
- SYNC character detection
- Leading SYNC character stripping.

In addition, the line units can perform the following functions:

- Modem control and monitoring
- Cyclic redundancy character testing
  - Zero bit stuffing
  - Zero bit stripping
- Automatic flag transmission
- Automatic flag recognition
- Automatic abort sequence transmission
- Automatic abort sequence recognition
- Automatic pad character transmission

## 1.4.2 Operating Modes

The line units can operate in either of two microprogrammable modes. The modes are:

1. **DDCMP Mode**—This is an 8-bit byte mode of operation. It is designed for the highly efficient byte-oriented Digital Data Communications Message Protocol (DDCMP) using the CRC-16 polynomial.
2. **Bit Stuff Mode**—This is a bit-oriented mode of operation. It is designed for the bit-oriented message protocols using the flag and abort sequences and the modified CRC-CCITT polynomial.

The line unit provides a data path between the microprocessor and a data set (or local link) and vice versa.

## 1.4.3 Microprocessor – Line Unit Data Path

The following discussion is keyed to the block diagram shown in Figure 1-1.

The microprocessor and line unit communicate through two unidirectional data paths. Signals ALU 0–7 comprise the data path from the microprocessor to the line unit. The line unit appears to the microprocessor as eight registers. The data is passed to the correct register by control signals CROM 0–3. Signal OBW is the strobe.

The line unit communicates with the microprocessor through the Line Unit In Bus (LU IBUS). The microprocessor controls all reading of the line unit registers.

Various maintenance signals are passed to the Maintenance and Miscellaneous logic. These signals control the functioning of the receiver and transmitter in the maintenance mode.

## 1.4.4 Transmitter

The transmitter portion of the line unit consists of three functional groups of logic. They are:

1. Out Data Silo
2. Transmitter Control
3. Transmitter CRC Logic

This logic performs specific parts of the transmission function. The functions are explained below.

The Out Data Silo is seen as a write only register to the microprocessor. The Transmitter Control logic sees it as a buffer. The silo is a 64-word deep data path between the microprocessor and the Transmitter Control logic.

The hardware implementation of this silo is through the use of First In/First Out (FIFO) devices. The silo effect is necessary because of the speed difference between the serialization process and the data available from the microprocessor. Because of the speed with which the microprocessor could load characters (conceivably, one character every 300 ns) and the speed at which the characters can be serialized (using dial up facilities, approximately one character every 160  $\mu$ s), there must be a multi-character buffer. Additionally, in order to relieve the microprogram of the need to have timers in order to know when to load another message or when to end a message, the transmitter control bits [Start of Message (SOM) and End of Message (EOM)] are siloed also.

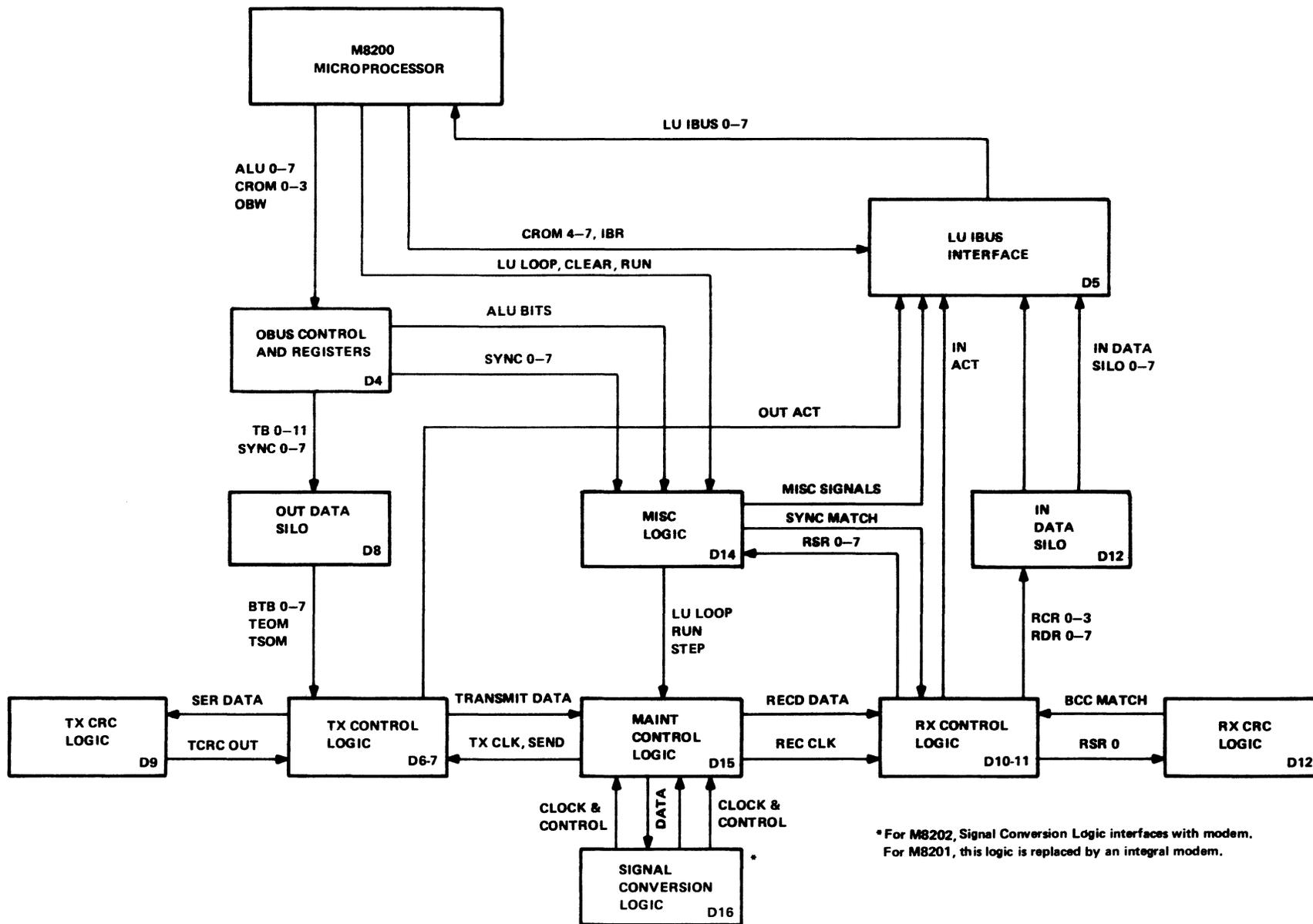


Figure 1-1 Line Unit Simplified Block Diagram

A typical sequence of operation is:

1. Microprogram loads SOM into the Out Control register.
2. Microprogram loads data into the Out Data Silo.
3. The transmitter detects SOM at the silo output.
4. Request to send is asserted by the transmitter, automatically.
5. Clear To Send and Data Set Ready come true.
6. The transmitter is enabled. Serialization begins.

As long as the SOM bit is true, the data being serialized is not included in the CRC computation.

When the Tx Control detects a character available from the silo without the SOM bit set, it includes that character, and all the characters following it, in the CRC computation.

When EOM is detected, the Tx Control transmits the CRC Check Character (called the BCC). If more data follows the EOM, a new CRC computation is begun.

#### **1.4.5 Receiver**

The receiver portion of the line unit consists of three functional groups of logic. They are:

1. In Data Silo
2. Receiver Control
3. Receiver CRC Logic

This logic performs specific parts of the receive function. The functions are explained in the following paragraphs.

The In Data Silo is seen by the microprocessor as a read only register. The Rx Control sees it as an output buffer. The silo is a 64-word deep data path between the Rx Control and the microprocessor.

The hardware implementation of the silo is similar to that used in the transmitter. Input to the In Data Silo is controlled by the Rx Control, while output is controlled by the microprogram. The silo is present for the same reasons mentioned in the discussion of the transmitter.

A typical sequence of operations is:

1. The receiver becomes active after detecting the first data character preceded by two or more synchronizing sequences (one flag sequence in the case of Bit Stuff mode).
2. The data character is included in the CRC computation automatically.
3. The data character is loaded into the silo by the Rx Control.
4. The microprogram detects (by bit testing) both In Active and In Ready (bits 6 and 4, respectively, of the In Control register).
5. The microprogram reads the In Data Silo.

6. The silo presents In Rdy with each subsequent character.
7. The microprogram, having determined when the message ends, checks the BCC Match bit (bit 0 of the In Control register). If the bit is set, the message had no detected errors.
8. In Bit Stuff mode, the Block End bit (bit 1 of R12) is set with the BCC Match bit, if no errors were detected.

#### **1.4.6 Signal Conversion and Maintenance Logic**

The signal conversion and maintenance logic provide automatic modem control, clock sources for the transmitter and receiver, and the receiver data source.

1

2

3

4

5

## CHAPTER 2 INSTALLATION

### 2.1 SCOPE

This chapter provides information for installation and checkout of the M8201 and M8202 Line Units.

### 2.2 UNPACKING AND INSPECTION

The line unit comes in four versions that are described below.

DMC11-DA (For EIA/CCITT V24 Interface)  
M8201 - Line Unit Module  
BC08R-1 or BC08S-1 - Interconnect Cable  
BC05C-25 - Modem Cable  
H325 - Test Connector

DMC11-FA (For CCITT V35 Interface)  
M8201 - Line Unit Module  
BC08R-1 or BC08S-1 - Interconnect Cable  
BC05Z-25 - Modem Cable  
H325 - Test Connector

DMC11-MA (Local 1M bps)  
M8202-YA - Line Unit Module  
BC08R-1 or BC08S-1 - Interconnect Cable  
12-12528 - Coaxial Test Connector

DMC11-MD (Local 56K bps)  
M8202-YB - Line Unit Module  
BC08R-1 or BC08S-1 - Interconnect Cable  
12-12528 - Coaxial Test Connector

Inspect these parts for visible damage. Report any damage or shortage immediately to the shipper and the DIGITAL representative.

### 2.3 PRE-INSTALLATION SETUP PROCEDURES

#### NOTE

The line unit cannot function without the DMC11-AD Microprocessor (M8200). It is assumed that the DMC11-AD has been installed and checked out in accordance with Chapter 2, Installation, of the *Microprocessor Manual* (EK-DMCUP-MM-001).

Before installing the line unit, check the jumpers and switches to be sure that they are in the normal configuration.

1. **Jumpers** - The M8201 Line Unit contains six jumpers (W1-W5). The M8202 Line Unit contains six jumpers (W1-W6). Refer to the components location drawing in the print set to locate the jumpers. The normal jumper configurations are described in Table 2-1 for the M8201 and Table 2-2 for the M8202.

**Table 2-1 M8201 Jumper Configurations**

Jumper Number	Normal Configuration	Function
W1	Installed	<p>With this jumper installed, the transmitter CRC character is not inverted by the CRC register output gate.</p> <p>This jumper must be in to ensure proper operation of codes CRC-16 and CCITT under the discipline of DDCMP and Bit Stuff protocols.</p> <p>If the user removes this jumper for some special reason, the Transmitter CRC character is inverted by the CRC register output gate. The diagnostic will fail also.</p>
W2	Installed	Jumpers W2 and W3 are used together.
W3	Removed	<p>With W2 installed and W3 removed, the modem Data Set Ready line controls the state of signal D16 MODEM RDY H.</p> <p>With W3 installed and W2 removed, signal D16 MODEM RDY H is always asserted. This feature accommodates modems that require Data Set Ready to be on continuously.</p>
W4	Installed	Jumpers W4 and W5 are used together.
W5	Removed	<p>With W4 installed and W5 removed, signal D15 DTR H controls the state of the modem Request to Send line.</p> <p>With W5 installed and W4 removed, the Request to Send line is on continuously. This feature accommodates modems that require this condition.</p>

**Table 2-2 M8202 Jumper Configurations**

<b>Jumper Number</b>	<b>Normal Configuration</b>	<b>Function</b>
W1	Installed	<p>With this jumper installed, the transmitter CRC character is not inverted by the CRC register output gate.</p> <p>This jumper must be in to ensure proper operation of codes CRC-16 and CCITT under the discipline of DDCMP and Bit Stuff protocols.</p> <p>If the user removes this jumper for some special reason, the Transmitter CRC character is inverted by the CRC register output gate. The diagnostic will fail also.</p>
W2, W3	Removed	When installed, the modem receiver protection transformer is disabled. Installation is not recommended.
W4, W5	Removed	When installed, the modem transformer protection is disabled. Installation is not recommended.
W6	Removed	Installed for 1-wire half-duplex operation only.

2. **Switch Packs No. 2 and No. 3** – Switch packs no. 2 and no. 3 are both eight switch DIPs. Switch pack no. 2 is Register 15 and is installed in location E87 on the M8201 Line Unit and in location E90 on the M8202 Line Unit. Switch pack no. 3 is Register 16 and is installed in location E88 on the M8201 Line Unit and in location E91 on the M8202 Line Unit.

When the line unit module is shipped, all switches in both packs are OFF. This is the default status (377).

These switches are a function of the down-line loading feature of the DMC11. After installation, the switches can be positioned to accommodate the user's requirements. For details, refer to Chapter 3 in the *Microprocessor Manual*.

3. **Switch Pack No. 1** – Switch pack no. 1 is an eight switch DIP that is installed in location E26 on the M8201 Line Unit and in location E29 on the M8202 Line Unit.

For the M8201, all switches except no. 5 are used. For the M8202, all switches except nos. 4, 5, and 8 are used. The ON and OFF positions and the switch numbers are marked on the package. The switches are the rocker type and are pushed to the desired position.

Table 2-3 describes the normal configuration for switch pack no. 1.

**Table 2-3 Configuration of Switch Pack No. 1**

Switch Number	Normal Position	Function
1	OFF	<p>With S1 OFF, signal D14 GRTP is low which enables the following ROMs.</p> <p>Transmitter Function Decode ROM            Transmitter Data Decode ROM            Receiver Decode ROM            Receiver Function ROM</p> <p>During servicing with the automatic module tester, if S1 is ON, signal D14 GRTP is high, which disables these ROMs.</p>
2	OFF	<p>With S2 OFF, signal D14 NO CRC is low, which allows the CRC function to be enabled.</p> <p>With S2 ON, the CRC function is inhibited.</p>
3	OFF	<p>With S3 OFF, signal D14 SEC MODE is low, which inhibits operation of the line unit in the secondary mode. This mode is applicable only in the Bit Stuff protocols.</p>
4	OFF	<p>With S4 OFF, Received Data, Modem Receive Clock, and Modem Transmit Clock are presented to the line unit through the EIA/CCITT V24 interface.</p> <p>With S4 ON, these signals are received through the CCITT V35 interface.</p> <p>This switch is used only on the M8201 Line Unit.</p>
5		Not used.
6	OFF	<p>Signal D14 SECURE is associated with this switch. It is bit 0 of the Modem Control register. This bit is reserved and is read only.</p>
7	Module Dependent	<p>Signal D14 SW is associated with this switch. It is read only bit 1 of the Modem Control register. It is read by the diagnostics and indicates the type of line unit.</p> <p>With an M8201 Line Unit, S7 should be ON (D14 SW is low).</p> <p>With an M8202 Line Unit, S7 should be OFF (D14 SW is high).</p>

**Table 2-3 Configuration of Switch Pack No. 1 (Cont)**

Switch Number	Normal Position	Function
8	ON	<p>With S8 ON, the internal RC clock is sent to the modem cable connector (J1) on the M8201 Line Unit.</p> <p>During servicing with the H325 test connector installed on the modem cable, the RC clock is sent back to the line unit as the transmit and receive clocks.</p> <p>During normal operation, the switch should remain ON.</p> <p>This switch is used only on the M8201 Line Unit</p>

**2.4 INSTALLATION AND CHECKOUT**

The M8201 and M8202 Line Units are hex modules. They do not interface with the Unibus so module edge connectors A and B are not required. As a result, the corner of the module in the vicinity of the A and B connectors has been removed. This allows the M8201 or M8202 to be installed in the end slots of the DD11-B, C, or D System Interfacing Units. The module plugs into connectors C, D, E, and F and fits over the Unibus cable connectors and short length (approximately 2-1/2 in.) Unibus terminator that are installed in connectors A and B.

Proceed with the installation and checkout as follows.

1. Install the M8201 or M8202 Line Unit.
2. Interconnect the line unit and the microprocess using cable BC08R-1 or BC08S-1 which is a 1-foot long 40 conductor flat mylar cable with H856 female connectors on each end. The mating connector on the microprocessor and line unit is an H854 male connector. On the microprocessor this connector is designated J1. On the M8201 Line Unit it is designated J2 and on the M8202 Line Unit it is J1.
3. On the M8201 Line Unit, install the BC05C-25 cable to connector J1. On the other end of this cable, connect the H325 test connector.

On the M8202 Line Unit, install the 12-12528 coaxial test connector that ties the two coaxial pigtailed together. These two 3-foot cables are soldered to the M8202.

4. Run MAINDEC-11-DZDME and -DZDMF to verify correct line unit operation.
5. Run MAINDEC-11 DZDMG to verify correct line unit/microprocessor system operation.
6. Remove the test connector from the line unit.

**M8201** – Connect the BC05C-25 Cinch connector to the customer supplied modem.

**M8202** – Connect the coaxial pigtailed to the customer supplied coaxial cables.

**CAUTION**

**The maximum allowable length for the BC05C or BC05Z cable is 50 feet.**

## 2.5 JUMPER AND SWITCH CHECKLIST

Table 2-4 represents a concise checklist of the M8201 and M8202 Line Unit switch settings and jumper configuration as shipped.

**Table 2-4 Jumper and Switch Checklist**

Jumper Configuration			
Jumper Designation	DMC11-DA M8201	DMC11-FA M8201	DMC11-MA/MD M8202
W1	IN	IN	IN
W2	IN	IN	OUT
W3	OUT	OUT	OUT
W4	IN	IN	OUT
W5	OUT	OUT	OUT
W6	NA	NA	IN FOR HD

**Settings For Switch Pack No. 1**

S1	OFF	OFF	OFF
S2	OFF	OFF	OFF
S3	OFF	OFF	OFF
S4	OFF	ON	OFF
S5	OFF	OFF	OFF
S6	OFF	OFF	OFF
S7	ON	ON	OFF
S8	ON	ON	OFF

**Settings for Switch Pack Nos. 2 and 3**

S1-S8	OFF	OFF	OFF
-------	-----	-----	-----

### NOTES

1. Switch Pack Locations

SP1-E26 on M8201 and E29 on M8202  
 SP2-E87 on M8201 and E90 on M8202  
 SP3-E88 on M8201 and E91 on M8202

2. All switches OFF in SP2 and SP3 represents the default status. Reference the *DMC11 Microprocessor Manual* for details on the use of these switches.

### 2.6 LOCAL LINK CABLE

This section discusses the selection, installation, and maintenance of the local link cable. This cable must serve two purposes. The link cable must deliver the generated signal to the receiver with sufficient amplitude to exceed the receiver threshold and it must shield the signal from external electrical noise.

### 2.6.1 Selection

For use in the DMC11, DIGITAL recommends the Belden 8232 double-shielded (triaxial) cable, or its equivalent. The electrical characteristics are listed below. The nominal specifications are given unless otherwise stated.

Inductance	0.097 $\mu$ H/ft (0.318 $\mu$ H/meter)
Capacitance	17.3 pF/ft (56.7 pF/meter)
Vel. of Prop.	78 percent
Impedance	75 $\Omega$
Attenuation (MHz)	dB/ft
1	0.25
10	0.8
50	1.8
100	2.7
Voltage Rating	175 Vrms
Sweep Test	22 dB min
Conductor dc Resistance	34.5 $\Omega$ /1000 ft (111.5 $\Omega$ /km)
Shield dc Resistance (each shield)	2.6 $\Omega$ /1000 ft (8.53 $\Omega$ /km)

The required physical characteristics are:

- Triaxial
- Cellular polyethylene insulation
- 20 AWG center conductor

The Belden 8232 cable meets all of these requirements. The cable provides the required 75  $\Omega$  match to the line unit transmitter and receiver circuits. Its double shield provides excellent noise rejection. The combination of the 20 AWG center conductor and cellular polyethylene dielectric provides low signal loss and distortion. The polyethylene jacket has excellent weather and abrasion resistance, very good chemical resistance, fair flexibility, and it does not contaminate the other dielectric. Other typical communications cable types (i.e., typical RG 59/u coax with 22 AWG conductor) using a solid polyethylene dielectric and single shield cannot be used for a 6000 foot connection.

When selecting cable, several factors must be considered in determining cable attenuation. The value given by the cable vendor is for room temperature and is nominal, being subject to deviation up to 20 percent. The attenuation increases with temperature at approximately 0.20%/° C (0.11%/° F). At 50° C (122° F) an additional loss of 5 percent over the room temperature specification can be expected. Finally, use at elevated temperatures causes aging at a faster than normal rate and, after five years, could produce yet another permanent 10 percent increase in attenuation. Thus the initial nominal 2.6 dB/1000 ft loss could become, after five years use at high temperature, 5.2 dB/1000 ft worst case.

## **2.6.2 Installation**

The characteristics of the local link cable should be measured prior to installation. In particular, there are two parameters that the user should measure and note for future reference. These are the propagation time delay, which can be measured with a pulse generator and an oscilloscope, and the dc resistance of the cable with the far end of the center conductor shorted to the inner shield. For the Belden 8232, these parameters can be expected to be nominally 1.30 ns/ft and 32  $\Omega$ /1000 ft. Once the cable is installed, and both ends, therefore, are not available at the same place, the latter parameter can still be measured easily, and the former can be measured by use of the time domain reflectometry (TDR) method described in Paragraph 2.6.3.

While installing the cable, make a complete map of its layout, showing the position of the cable with respect to buildings, equipment and so forth, and also the locations of all access points, including not only splices and in-line connectors, but also pull boxes. Carefully measure and record cable lengths between landmarks. Such a map will facilitate maintenance greatly.

The user must take the following factors into account when installing the local link cable.

**TEMPERATURE** – The polyethylene used as the dielectric material in most coaxial and triaxial cables begins to soften above 80° C. As the conductor moves off center, variations in cable characteristics occur. If installed under tension with sharp bends, the conductor may short to the shield. Additionally, the open circuit resistance should be measured after installation to ensure against shorts incurred during installation. This resistance should be  $\geq 20$  k $\Omega$ . The closed circuit resistance should be 36.1  $\Omega$ /ft.

**MOISTURE** – Moisture or moisture-related impurities may enter the cable through cuts or scratches in the outer jacket or through improperly installed connectors. Minute amounts of water vapor will condense into water, which can migrate along the braid. Water condensed from a polluted atmosphere can contaminate the entire length of cable, shorten its lifetime, and seriously degrade performance.

**PULLING TENSION** – For most environmental conditions it is generally preferred that the cable be installed in conduit, through which the cable must be pulled. During installation, the total pulling tension on the 20 AWG center conductor must not exceed 12 pounds (8N).

For ease in maintenance, it is best to divide the cable into sections. For long cable runs in conduit, it is convenient to have a pull box every 100 feet or equivalent. A 90 degree conduit bend is equal to 30 feet of straight level conduit. It is recommended that an antifricition agent be used during pulling, provided the agent is compatible with the cable jacket material.

**SPLICES AND CONNECTORS** – The cable layout should provide access points for test purposes and for replacing defective sections (Paragraph 2.6.2.2). Strain relief must be provided at all splices and in-line connectors.

**RECOMMENDED WIRING PRACTICES** – Chapter 8, Article 800, of the *National Electric Code* defines wiring rules for communications circuits. These rules must be observed for safe operation of the DMC11. In particular, note these provisions of the code:

“Communication conductors shall not be placed in a raceway, compartment, outlet box, junction box or similar fitting with conductors for light and power. . .”

“Communication conductors may be run in the same shaft with conductors for light and power provided the conductors of the two systems are separated by at least two inches.”

“Suitable protective devices must be employed for wiring between buildings.”

**SURGE WITHSTAND CAPABILITY** – The receiver has no provision for protection against normal mode voltage surges exceeding 30 V. If surge withstand is required, the user must install a separate circuit to condition signals to the receiver.

**NOISE** – The M8202 is designed to operate with a common mode rejection ratio  $\geq 500:1$ . Cable selection, installation grounding, and noise suppression are means of reducing line error rates.

**2.6.2.1 Connectors** – The following components are recommended for use in joining cable sections and for connecting the cable to the M8202 pigtails. These components are manufactured by AMP Inc., Harrisburg, Pennsylvania.

<b>Component</b>	<b>DIGITAL Part No.</b>	<b>AMP Part No.</b>
Cable clamp	12-11430	206062-1
Male housing	12-12527	206152-1
Male pin	12-12001	66536-2
Female housing	12-12526	206060-1
Female pin	12-12000	66594-2

The connectors are installed by crimping the pins to the cable; the recommended crimper is the AMP Type V1, 90293-1. It is very unlikely that one can install a set of connectors without requiring the use of an ejector, to remove pins that have been inserted incorrectly; the proper ejector for the above pins is the AMP 305183.

The pin holes in the housing and receptacle are numbered. When working with a connector, always orient it so that hole 1 is at the top, then hole 4 is at the bottom, and the holes on either side are 2 and 3.

1. The cable clamp assembly is supplied as a shell, two screws, and three clamps, of which the one for the largest cable size should be used. Slide the shell onto the cable.
2. Dress the center conductor back enough so it will fit into a pin with the pin crimped to its insulation as well as to the conductor. Dress both shields back about another 1/2 inch, and taper the final 1/2 inch of the inner insulation so that its tip fits into the pin, and about 1/4 inch fits into the connector, along with the center conductor. Crimp the pin to both the conductor and its insulation, and insert the pin in hole 1.
3. Separate the inner shield into two parts, attach pins to them, and insert the pins into holes 2 and 3.
4. Pull the outer shield together, insulate it from the inner shield, crimp a pin to it, and insert the pin in hole 4.
5. Screw the shell into the housing, and screw the clamp to the shell.
6. After male and female connectors have been plugged together, screw the other ring of the female housing over the male housing.

Both M8202 pigtails have female connectors; therefore, the local link cable must have a male connector. The connectors at the ends of the cables are installed in the same manner previously described except that the outer shield must be grounded at the ends as described in Paragraph 2.6.2.2. The male connector is made up for the computer connection. The wire protruding from the back end of the connector is the outer shield.

**2.6.2.2 Grounding** – The outer braided shield of the cable must be grounded near, but not to, the computer system chassis. The grounding conductor should be connected to a water pipe electrode or, if none is available, to the power service conduit, service equipment closure, or grounding electrode conductor where the grounding conductor of the power service is connected to a water pipe electrode at the building.

When neither of these means of grounding is available, it is permissible to connect the grounding conductor to the service conduit, service equipment enclosure, grounding electrode conductor, or grounding electrode of the power service of a multigrounded neutral power system.

If it is impossible to ground the cable shield by one of the above methods, connect the grounding conductor to one of the following:

1. A concrete-encased electrode of not less than 20 feet of bare copper conductor, no smaller than 4 AWG, encased in at least 2 inches of concrete, and located within and near the bottom of a concrete foundation footing that is in direct contact with the earth.
2. An effectively grounded metal structure.
3. A continuous and extensive underground gas-piping system, where acceptable to both the servicing gas supplier and to the authority having jurisdiction.
4. A ground rod or pipe driven into permanently damp earth.

**WARNING**

**Under no circumstances shall the grounding conductor be connected to a steam or hot water pipe, a lightning rod conductor, or pipe or rod electrodes grounding other than multiground neutral power circuits.**

**2.6.3 Maintenance**

For maintenance purposes, the user should keep a record of the initial cable characteristics, particularly the propagation time delay and short circuit line resistance as indicated at the beginning of Paragraph 2.6.2. Once the system is operational, record the received signal amplitude at the M8202. Then repeat this measurement at every scheduled preventive maintenance (PM) date (at least four times per year). If a deviation of 20 percent is observed in the signal amplitude, disconnect both ends of the cable from the M8202 and measure both the open circuit and short circuit resistance of the line. If the measured open circuit resistance is less than 20 M $\Omega$ , inspect the cable for contamination of the dielectric and for adverse effects of sharp bends or stress points, elevated temperatures, or aging. If the line resistance with a shorted end increases above the value measured at installation, inspect the cable for loose connectors, contaminated connectors, and excessive tension.

**LOCATING A DEFECTIVE SECTION** – An ohmmeter can be used to diagnose an open line or a low impedance shorted line, by checking one section at a time until the faulty section is located. If the cable is not partitioned into small enough sections, the distance to the fault can be measured by making use of TDR.

Although TDR cable testers are available from Tektronix and others, a pulse generator and oscilloscope can be used for approximate measurements. Disconnect both ends of the cable, and drive one end with a 5 V peak, 100 ns wide pulse with a repetition rate below 10 kHz. Measure the time interval between the leading edge of the driven pulse and the leading edge of the first reflection. The reflected pulse will be in the 10 mV to 1 V range. It will be normal for a line open, but inverted for a line short. Figure 2-1 shows typical oscilloscope traces for both cases. The time interval represents the propagation time delay for a round trip from the signal generator to the fault and back again. The distance D to the fault in feet (meters) is

$$D = T_p/2p$$

where  $T_p$  is the measured time delay in nanoseconds, and p is the propagation time in nanoseconds per foot (meter) recorded before the cable was installed.

## 2.7 FULL-DUPLEX/HALF-DUPLEX OPERATION

The DMC11 is capable of either full-duplex or half-duplex operation. The microprogram controls the transmitter-receiver interaction in half-duplex mode in order to minimize the line control contention problems.

While there are few considerations required when selecting half-duplex operation of the DMC11-DA or DMC11-FA Units, careful thought should be given to the selection of full- or half-duplex operation of the DMC11-MA/DMC11-MD Line Units.

Full- or half-duplex operation of the DMC11-DA/FA requires selecting the proper data set and informing the microprogram that half-duplex mode has been selected.

Operation of the DMC11-MA/MD Line Units requires hardware considerations. Full-duplex operation requires two separate local link cables. Half-duplex operation requires only one. The two cable requirement for full-duplex operation cannot be eliminated through the use of a dual coax/triax cable.

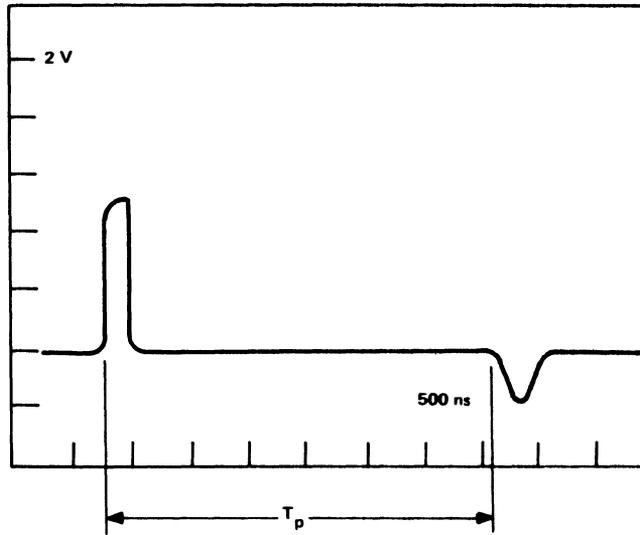
While full-duplex operation requires two cables, it also provides full throughput potential. Half-duplex operation implies half the throughput potential, but requires only one cable. The following factors should be considered when selecting full-duplex or half-duplex operation.

1. Traffic Flow - Is most of the data going one way or is data flow nearly equal in both directions?
2. Data Rate - Is it necessary to use maximum data rate now and in the foreseeable future?
3. Cable Expense - Is the two cable full-duplex operation worth the expense?

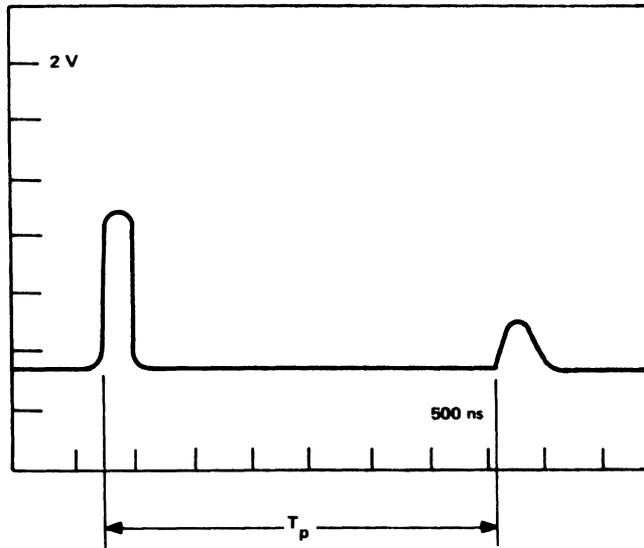
The local link line units (DMC11-MA/MD) require installation of the W6 jumper for half-duplex operation. This allows either line unit pigtail to be used as the output connection to the local link cable.

The connection to the local link cable is made so that the local transmitter pigtail is connected to the distant receiver pigtail through the local link cable (Figure 2-2).

In the case of half-duplex operation, the connection to the local link cable is made with either of the pigtails (Figure 2-2).



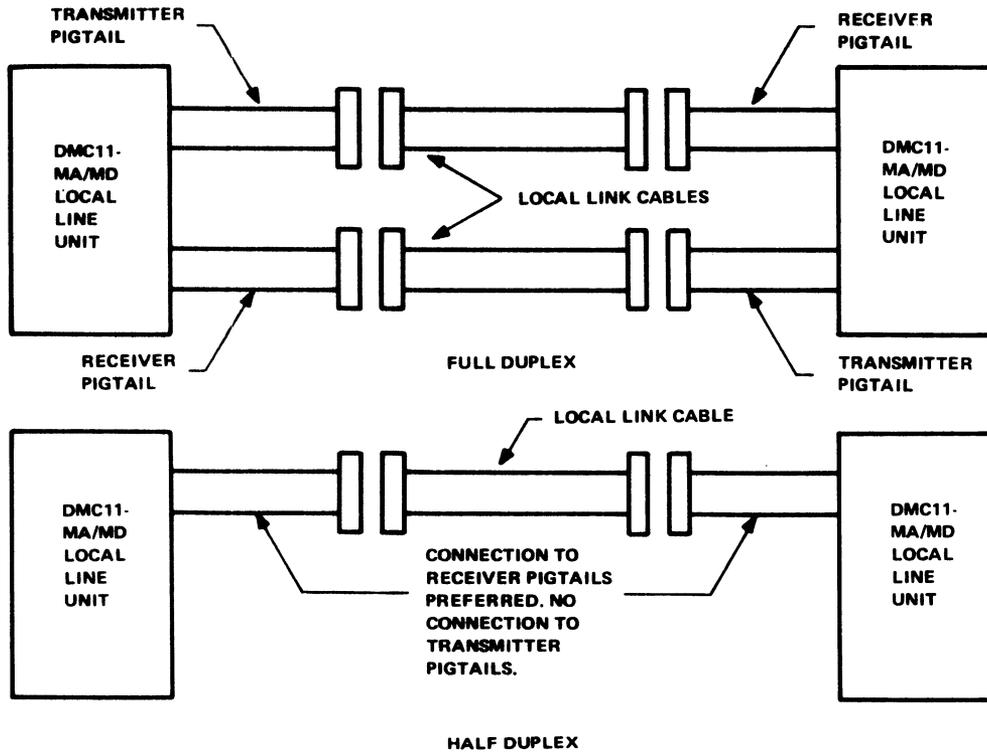
SHORTED LINE



OPEN LINE

11 - 4452

Figure 2-1 Signal Reflections from a Line Fault



11 - 4415

Figure 2-2 Full-Duplex/Half-Duplex Connections

1

2

3

4

5

## CHAPTER 3 PROGRAMMING

### 3.1 INTRODUCTION

This chapter contains general programming information. It is divided into two sections: one lists the register bit functions and the other discusses programming procedures.

### 3.2 REGISTERS AND DEVICE ADDRESS SELECTION

The nine registers used in the line unit are shown in Table 3-1. They are all 8 bit registers.

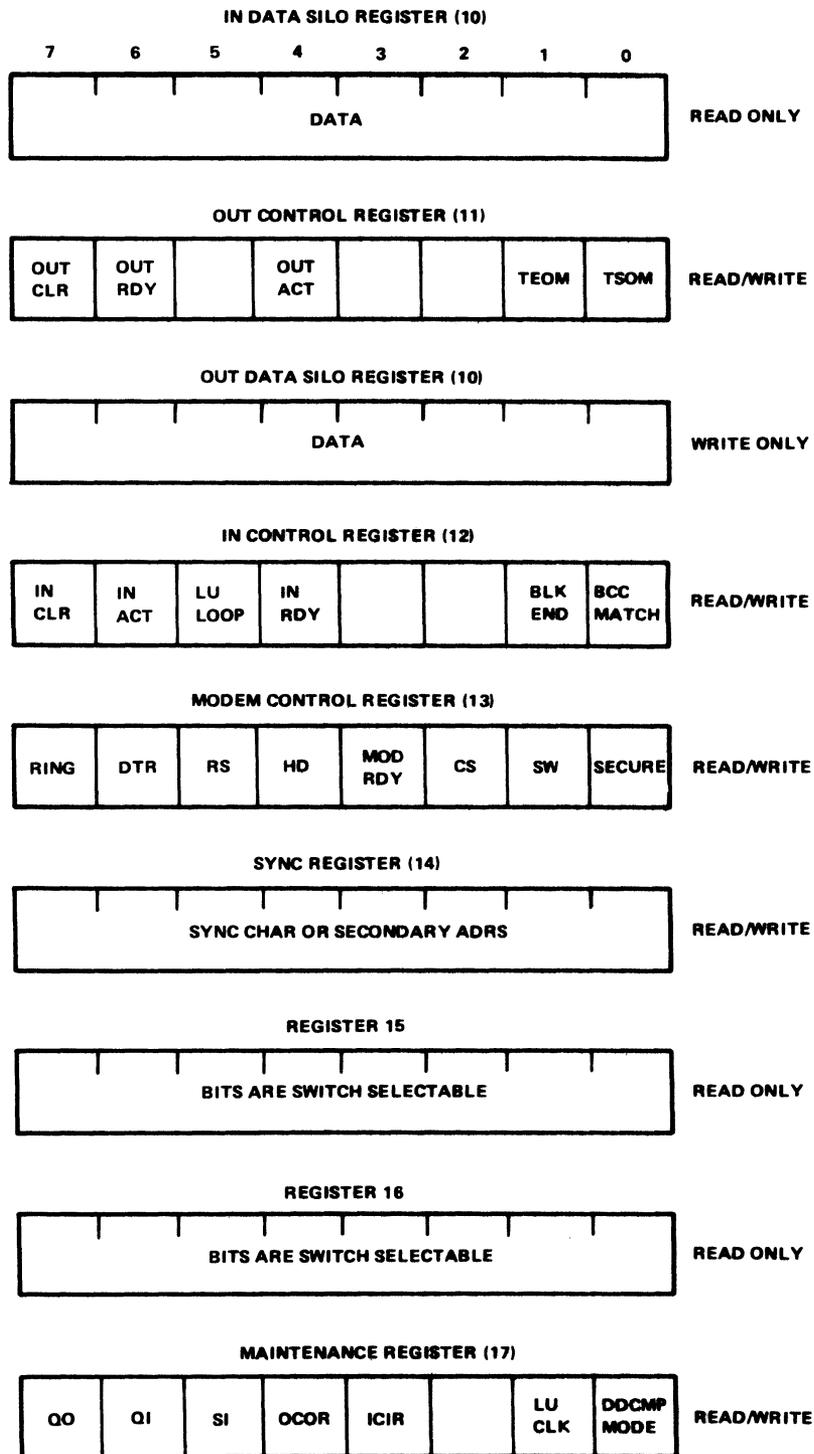
Table 3-1 Line Unit Registers

Name	Address	Comments
In Data Silo	10	Read only
Out Data Silo	10	Write only
Out Control Register	11	Read/write
In Control Register	12	Read/write
Modem Control Register	13	Read/write
Sync Register	14	Read/write
Register 15	15	Bits are switch selectable Read only
Register 16	16	Bits are switch selectable Read only
Maintenance Register	17	Read/write

The DMC11 (microprocessor plus line unit) is assigned a device address in the floating address space, which includes addresses 7600010 through 764000. The device address selection logic is located physically on the microprocessor module. The line unit registers are selected by four address signals from the microprocessor.

### 3.3 REGISTER BIT ASSIGNMENTS

Bit assignments for all the registers are shown in Figure 3-1. If applicable, the register is described by showing a bit assignment illustration and an accompanying table that discusses each bit in detail.



11 - 4416

Figure 3-1 Line Unit Register Configurations and Bit Assignments

The cable that connects the line unit and the microprocessor contains two buses. The IN BUS (IBUS) carries information from the line unit to the microprocessor. The OUT BUS (OBUS) carries information from the microprocessor to the line unit.

### 3.3.1 Data Silo Registers

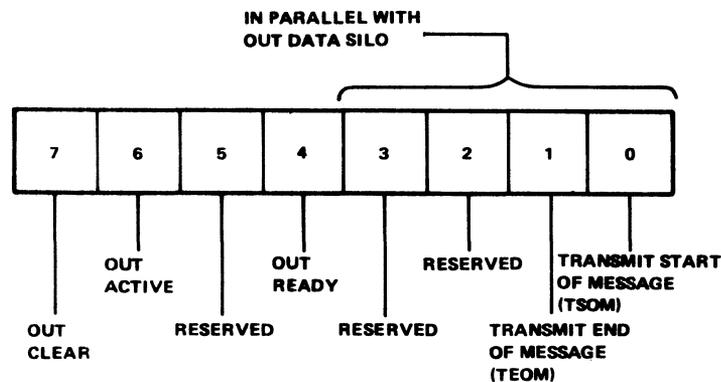
The line unit contains two Data Silo registers. They are the In Data Silo, which is read only, and the Out Data Silo, which is write only. The two buses (In Bus and Out Bus) that interconnect the line unit and microprocessor allow these registers to share the same address (10 octal). When register 10 is selected on the In Bus, the data in the In Data Silo is read by the microprocessor. This is an 8-bit data character from the receiver. When register 10 is selected on the Out Bus, the microprocessor writes data into the Out Data Silo. This is an 8-bit data character to be transmitted.

Both silos are  $64 \times 12$  bit FIFOs. The In Data Silo and Out Data Silo each contain 8 bits (0-7 of the silo). In each case, the remaining four bits (8-10) belong to another register. For the In Data Silo, these are bits 0-3 of the In Control register (11 octal). For the Out Data Silo, these are bits 0-3 of the Out Control register (12 octal).

In Control register bits 0-4 are updated every time register 10 is read. Therefore, they must be read before register 10 is read or they will be lost.

Out Control register bits 0-4 are passed to the transmitter through the silo every time register 10 is written into. Therefore, if control information is to be passed, these bits must be written into before register 10 is written into.

### 3.3.2 Out Control Register (Figure 3-2)



**NOTE:**

Bits 0-3 are passed to the transmitter through the silo every time register 10 is written into. Therefore, if control information is to be passed, these bits must be written into before register 10 is written into.

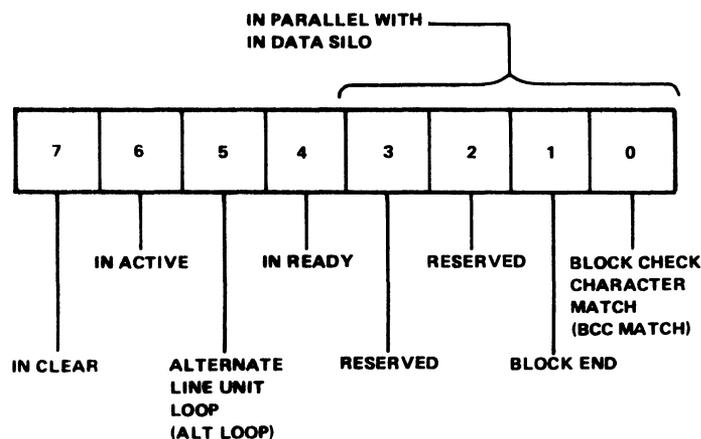
11 - 4417

Figure 3-2 Out Control Register Format

Bit	Name	Description
0	<p><b>TSOM</b> (Transmit Start of Message)</p>	<p>This bit is used to initiate the start of a new message.</p> <p><b>DDCMP Mode:</b> The Sync character must be loaded into the Out Data Silo along with the TSOM bit. This character is transmitted as the Sync character until TSOM is cleared. Until it is cleared, the characters are not included in the CRC accumulation. When TSOM is cleared, the present Sync character is transmitted and is followed by data. All data is included in the CRC accumulation, if CRC is enabled. Once TSOM has been set, the CRC accumulation cannot be inhibited unless the line unit is initialized.</p> <p><b>Bit Stuff Mode:</b> When TSOM is set, a flag character is automatically transmitted. The character that is loaded with the TSOM bit is lost. Flag characters are automatically transmitted as long as TSOM is set. When data is to be transmitted, TSOM is cleared and data is loaded into the Out Data Silo. At the completion of the current flag character, the actual transmission of data begins. All information to be transmitted is included in the CRC accumulation, if the CRC function is enabled.</p> <p>This bit is program write only. It is cleared by the initialization logic and by the fact that data was loaded into the Out Data Silo. This bit is loaded into the silo and passed to the transmitter through the silo.</p>
1	<p><b>TEOM</b> (Transmit End of Message)</p>	<p>This bit is used to terminate the message in progress and control the transmission of the CRC character, if the CRC function is enabled.</p> <p><b>DDCMP Mode:</b> When TEOM is set, the CRC character is transmitted. If no more messages are pending (TSOM cleared), the transmitter is shut down.</p> <p><b>Bit Stuff Mode:</b> When TEOM is set, the character loaded with it is lost. The CRC character is transmitted. If no more messages are pending, the transmitter is shut down by having a second TEOM in the silo. This generates a single terminating or inter-message flag.</p> <p>This bit is program write only. It is cleared by the initialization logic and by the TSIP flip-flop, which is set whenever data is loaded into the Out Data Silo. This bit is loaded into the silo and passed to the transmitter through the silo.</p>

Bit	Name	Description
2, 3	Reserved	These bits are program write only. They are cleared by the initialization logic and by the TSIP flip-flop, which is set whenever data is loaded into the Out Data Silo.
4	OUT RDY (Out Ready)	When asserted, this bit informs the microprocessor that the transmitter is ready to accept data. It indicates that space is available in the Out Data Silo. The microprocessor loads the Out Data Silo and then reads OUT RDY. The speed of the microprocessor allows OUT RDY to be read and interpreted as true before the silo has loaded the data. Therefore, one cycle must elapse between loading the silo and reading OUT RDY.  This bit is read only.
5	Reserved	Read only. This bit is switch selectable.
6	OUT ACTIVE	OUT ACTIVE informs the microprocessor of the status of the transmitter. When it is set, the transmitter is active.  This bit is read only. It is set by the hardware and cleared by the initialization logic.
7	OCLRP (Out Clear)	This bit is used to clear all the transmitted functions. OCLRP is program write only.

### 3.3.3 In Control Register (Figure 3-3)



**NOTE:**

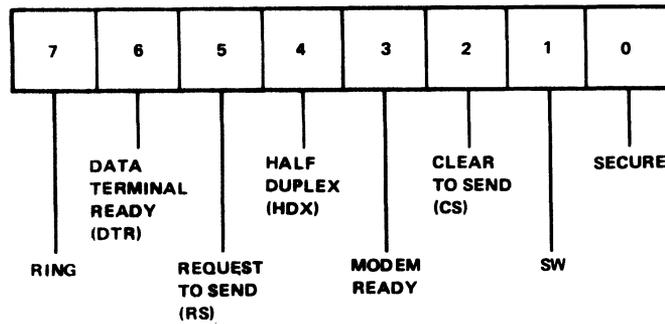
Bits 0-3 are updated every time register 10 is read. Therefore, they must be read before register 10 is read or they will be lost.

11 - 4418

Figure 3-3 In Control Register Format

Bit	Name	Description
0	BCC MATCH (Block Check Character Match)	<p>BCC MATCH is the output of the receiver CRC error logic that monitors the contents of the CRC register. With the CRC function enabled, BCC MATCH is asserted at the end of an errorless message. In the DDCMP protocol, the contents of the Receiver CRC register equal zero when an errorless message has been received. In the SDLC protocol, the contents of the Receiver CRC Register equal 016417.</p> <p>This bit is read only and is updated every time register 10 is read.</p>
1	BLOCK END	<p>BLOCK END is used to inform the microprocessor, in SDLC mode, that a terminating flag has been received. This flag may be the leading flag for the next message. The BLOCK END bit is loaded with the high byte of the CRC character; therefore, the BLOCK END bit along with the BCC MATCH bit should be used to indicate reception of a good message.</p> <p>This bit is read only and is not used in the DDCMP mode. It is updated every time register 10 is read.</p>
2, 3	Reserved	Read only.
4	IN RDY (In Ready)	<p>When asserted, this bit informs the microprocessor that received data is ready for processing. It indicates that data is available at the output of the In Data Silo.</p> <p>This bit is read only.</p>
5	ALT LU LOOP (Alternate Line Unit Loop)	<p>During maintenance, this bit is set to loop the receiver on the transmitter with no connection to the modem control lines.</p> <p>This bit is program read/write.</p>
6	IN ACTIVE	<p>When asserted, this bit informs the microprocessor that the receiver is in the data reception mode; that is, it is receiving data or CRC characters.</p> <p>DDCMP Mode: IN ACTIVE is asserted upon receipt of the first non-sync character.</p> <p>SDLC Mode: IN ACTIVE is asserted upon receipt of the first data character.</p>
7	ICLRP (In Clear)	<p>This bit is used to clear all the receiver functions.</p> <p>ICLRP is program write only.</p>

### 3.3.4 Modem Control Register (Figure 3-4)



11 - 4419

Figure 3-4 Modem Control Register Format

Bit	Name	Description
0	SECURE	The function of this bit is reserved for future use. This read only bit is selected by a switch. SECURE is asserted when the switch is OFF (open).
1	SW	The function of this bit is reserved for future use. This read only bit is selected by a switch. SW is asserted when the switch is OFF (open).
2	CS (Clear to Send)	The CS bit informs the microprocessor of the state of the modem Clear to Send line. This bit and MODEM RDY (bit 3) must be asserted simultaneously to generate SEND, which is the transmitter enabling signal.  This bit is read only.
3	MODEM RDY (Modem Ready)	The MODEM RDY bit informs the microprocessor of the state of the Modem Ready line. On the M8201 Line Unit, this signal can be held asserted permanently through the use of a jumper. On the M8202 Line Unit, this signal is asserted when power is turned on.  This bit is read only.
4	HDX (Half-Duplex)	The HDX bit is used to put the line unit in the half-duplex mode. When this bit and the Request to Send bit are asserted, the receiver clock is inhibited, which blinds the receiver during operation in the half-duplex mode.  This bit is program read/write and can be directly cleared by the clear signal from the microprocessor.

Bit	Name	Description
5	RS (Request to Send)	The RS bit informs the microprocessor of the state of the modem Request to Send line. This bit is controlled by the line unit logic and not by the microprocessor. It is cleared by absence of data or by the initialization logic.  This bit is read only.
6	DTR (Data Terminal Ready)	The DTR bit enables the modem via the Data Terminal Ready line. This bit is program read/write. It is directly set by the initialization logic but it can be cleared only by writing a 0 into it.
7	RING	The RING bit informs the microprocessor of the state of the modem Ring line. RING is inhibited on the M8202 Line Unit.  This bit is read only.

### 3.3.5 Sync Register

The Sync register is an 8-bit program read/write register.

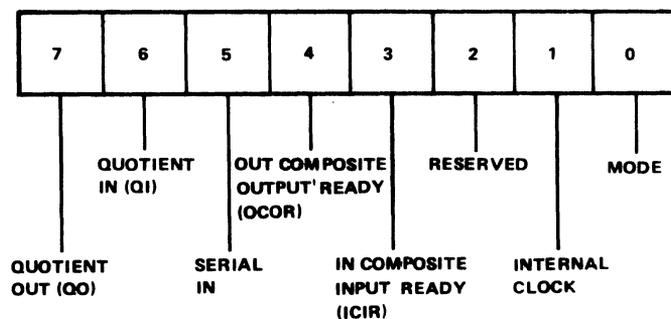
DDCMP Mode: The register is loaded with a program selectable sync character.

SDLC Mode: In the secondary mode, this register is loaded with the secondary station address. This 8-bit character follows the initial flag in the SDLC message format.

### 3.3.6 Switch Selectable Registers (R15 and R16)

Both of these registers are DIPs containing eight switches each. The program determines the function of both registers.

### 3.3.7 Maintenance Register (Figure 3-5)



11 - 4420

Figure 3-5 Maintenance Register Format

Bit	Name	Description
0	MODE	<p>The MODE bit selects the protocol (DDCMP or SDLC families). When set, DDCMP is selected; when cleared, SDLC is selected.</p> <p>During initialization, the CLEAR signal from the microprocessor sets this bit to select DDCMP. This bit can be cleared (SDLC selected) only by writing a 0 into it.</p> <p>This bit is read/write.</p>
1	ECS (Internal Clock)	<p>ECS is the output of the internal RC clock (approximately 10 kHz).</p> <p>This bit is read only.</p>
2	Reserved	Read only.
3	ICIR (In Composite Input Ready)	<p>When asserted, this bit indicates that the In Data Silo is ready to accept data.</p> <p>This bit is read only.</p>
4	OCOR (Out Composite Output Ready)	<p>When asserted, this bit indicates that data is ready at the output of the Out Data Silo.</p> <p>This bit is read only.</p>
5	SI (Serial Input)	<p>SI is the serial input data from the modem.</p> <p>This bit is read only.</p>
6	QI (Quotient In)	<p>QI is the least significant bit of the Receiver CRC register.</p> <p>This bit is read only.</p>
7	QO (Quotient Out)	<p>QO is the least significant bit of the Transmitter CRC register.</p> <p>i This bit is read only.</p>

### 3.4 PROGRAMMING PROCEDURES

The following programming procedures must be used to ensure proper operation of the line unit.

1. **Transmit Start of Message (TSOM) and Transmit End of Message (TEOM)** are bits 0 and 1 of the **Out Control register**. **TSOM** and **TEOM** are loaded into this register by the microprocessor. These bits are sent from the **Out Control register** to the **Transmitter Buffer** when the microprocessor loads a character (sync, data, etc.) into the **Out Data Silo register**. If set, the control bit (**TSOM** or **TEOM**) goes along with the character. However, the **Load** signal for the **Out Data Silo** also clocks the **TSIP flip-flop**, which clears the **TSOM** and **TEOM** bits in the **Out Control register**.

Therefore, always load the **TSOM** or **TEOM** bit into the **Out Control register** before loading the **Out Data Silo**. The control information is cleared from this register automatically as the **Out Data Silo** accepts the data.

2. In the **SDLC mode**, the data written into the **Out Data Silo** with either **TSOM** or **TEOM** is lost. This is an internal function that is performed automatically by the transmitter control logic. Physically, this is accomplished by inhibiting the loading of the **Transmitter Data Shift register**.

In place of the shift register output, the transmitter control logic transmits a flag character when **TSOM** is set and it sends the transmitter **CRC check character** when **TEOM** is set. If both **TEOM** and **TSOM** are set, 16 zeros are sent.

3. **BCC MATCH** and **BLOCK END** are bits 0 and 1 of the **In Control register**. Physically, they are part of the 3341 **FIFOs** that constitute the **In Data Silo**. When the 8 data bits of the **In Data Silo** are read by the microprocessor, **BCC MATCH** and **BLOCK END** are lost. These bits are read as part of the **In Control register**.

Therefore, always read the **In Control register** before reading the **In Data Silo**.

4. In the **DDCMP mode**, the **BCC MATCH** flag is presented with the **CRC check character** that produced the match information.

In the **Bit Stuff mode**, the **BLOCK END** bit is asserted when the terminating flag has been received. This bit is loaded with the high byte of the **CRC check character**. Therefore, the **BCC MATCH** bit along with the **BLOCK END** bit should be used to indicate reception of an errorless message.

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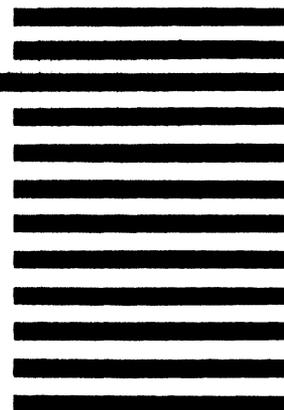
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