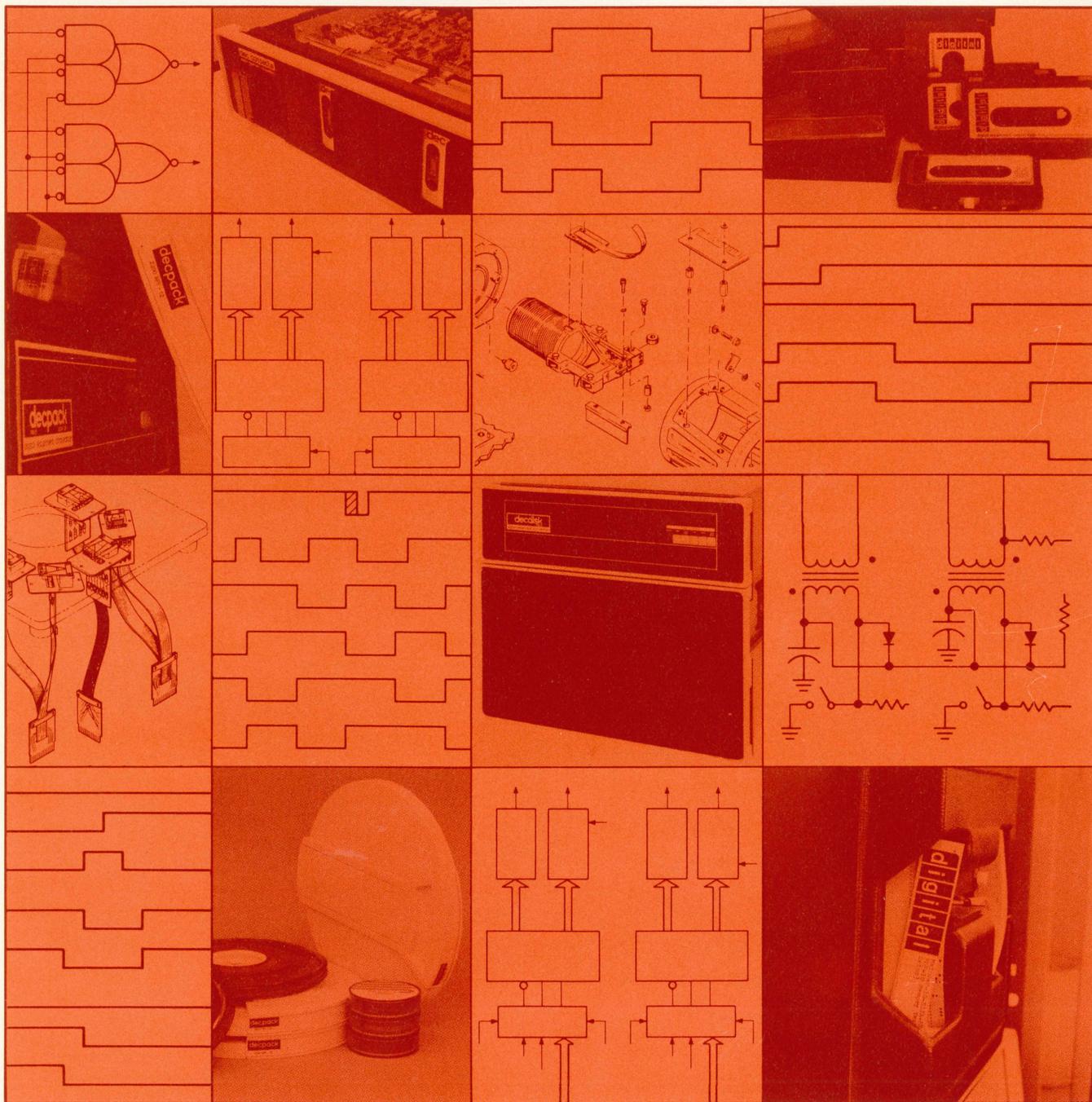


# digital

RP04 device  
control logic  
user's manual





**RP04 device  
control logic  
user's manual**

**EK-RP04-OP-001**

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## CHAPTER 1 INTRODUCTION

### 1.1 GENERAL

This manual describes the Device Control Logic (DCL) incorporated in the RP04 Disk Drive. The RP04 is divided into two major functional parts (Figure 1-1):

1. The DCL which houses the necessary logic circuits to interpret and implement all commands executable by the RP04 and allows for access by two different controllers.
2. The DEC 773 Disk Storage Drive which houses the circuits for: rotating the disk pack, positioning the read/write heads at the addressed cylinder track and sector; and writing/reading bits on the disk pack surface.

The DCL is capable of handling data transfers in either 16 or 18-bit format making the RP04 compatible with the PDP-11, PDP-15, and DECsystem-10. Each system has its own specialized controller that interfaces the RP04 with the related processor.

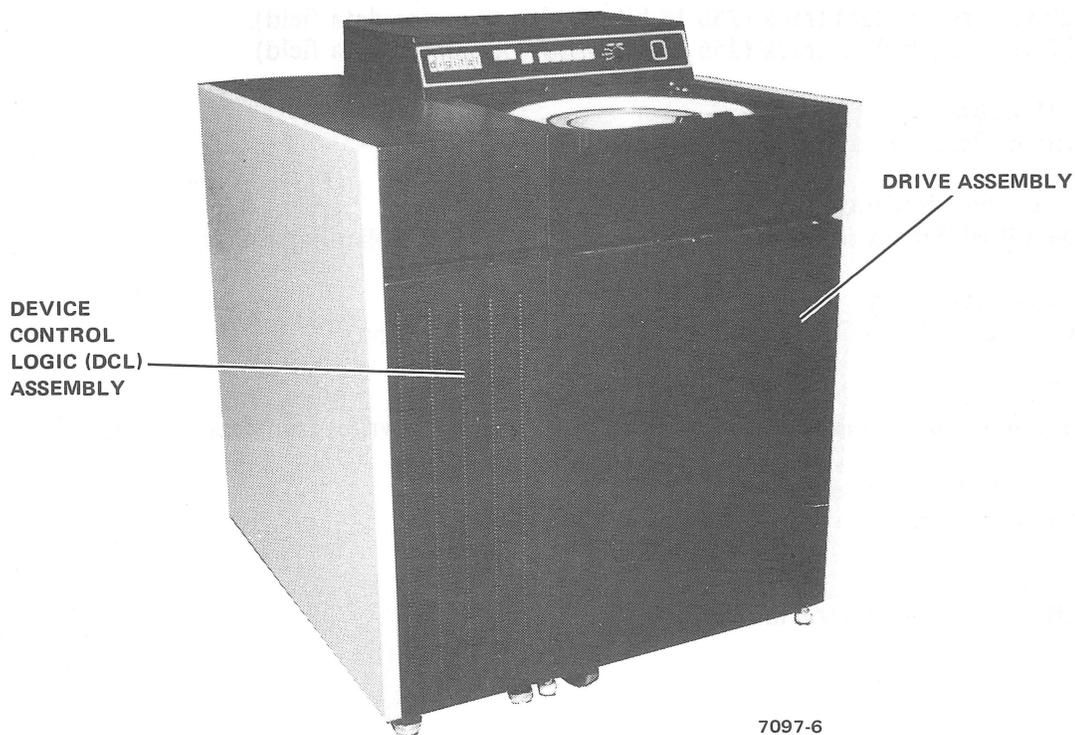


Figure 1-1 RP04 Drive and DCL Assemblies

# CHAPTER 1

## INTRODUCTION

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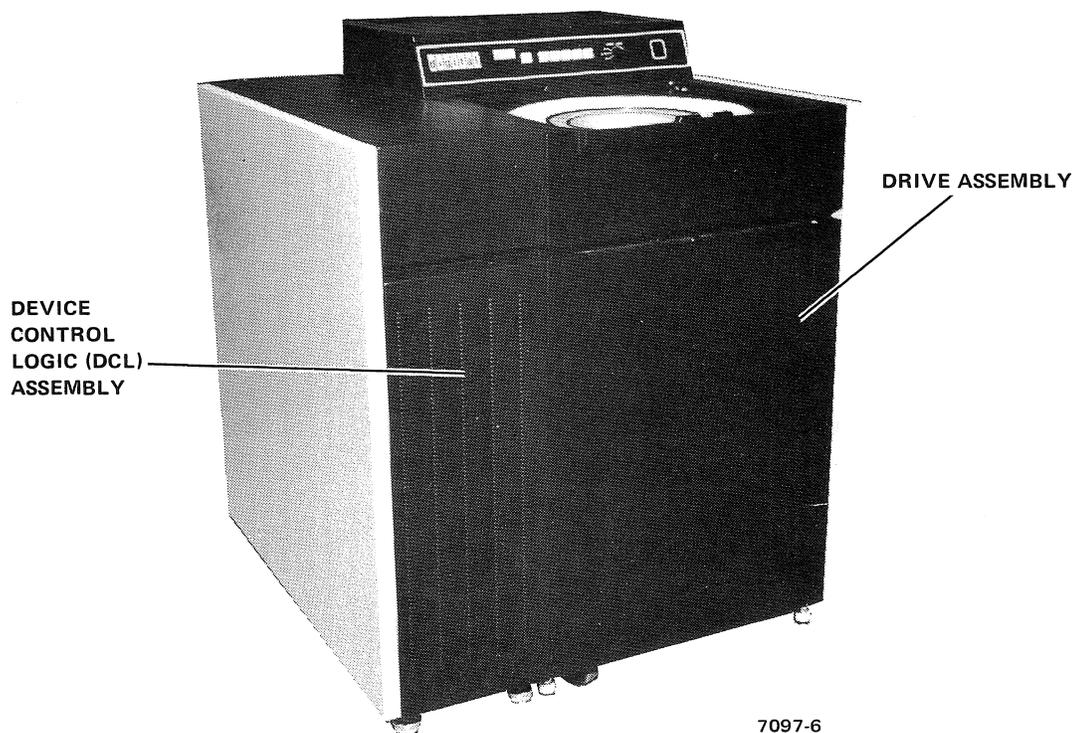


Figure 1-1 RP04 Drive and DCL Assemblies

## 1.2 APPLICABLE INSTRUCTION MANUALS

Instruction manuals bearing upon use of the RP04 depends on whether the device is configured in a PDP-11 or PDP-10 system environment (or both). When used with the PDP-11, applicable instruction manuals are:

- RP04 Disk Drive Installation Manual
- Model 733 DEC Disk Storage Drive Operation, Service and Diagrams Manual
- RJP04 Moving Head Disk Drive Maintenance Manual
- RH11 Controller Instruction Manual
- RP04 DCL Print Set

When the RP04 is used with the PDP-10 system, related handbooks are:

- RP04 Disk Drive Installation Manual
- Model 773 DEC Disk Storage Drive Operation, Service and Diagrams Manual
- RH10 Controller Instruction Manual
- RP04 DCL Print Set

## 1.3 SPECIFICATIONS

Data Format Option:

- 20 sectors per data track (256 18-bit words per sector data field).
- 22 sectors per data track (256 16-bit words per sector data field).

Error Handling:

Error Detection and Correction Capability.

Interface Characteristics:

MASSBUS Controller to device interface Dual Controller capability.

System Compatibility:

Can be used in PDP-11 or PDP-10 system configuration.

Data Transfer Modes:

Single sector or multisector (spiral or extended read/write) transfers.

Operating Temp. Ranges:

15° C minimum to 32° C maximum.

Humidity Range:

20% minimum to 80% maximum.

**Dimensions:**

9-inch wide by 35-inch high by 32-inch deep.

**Weight (DCL only):**

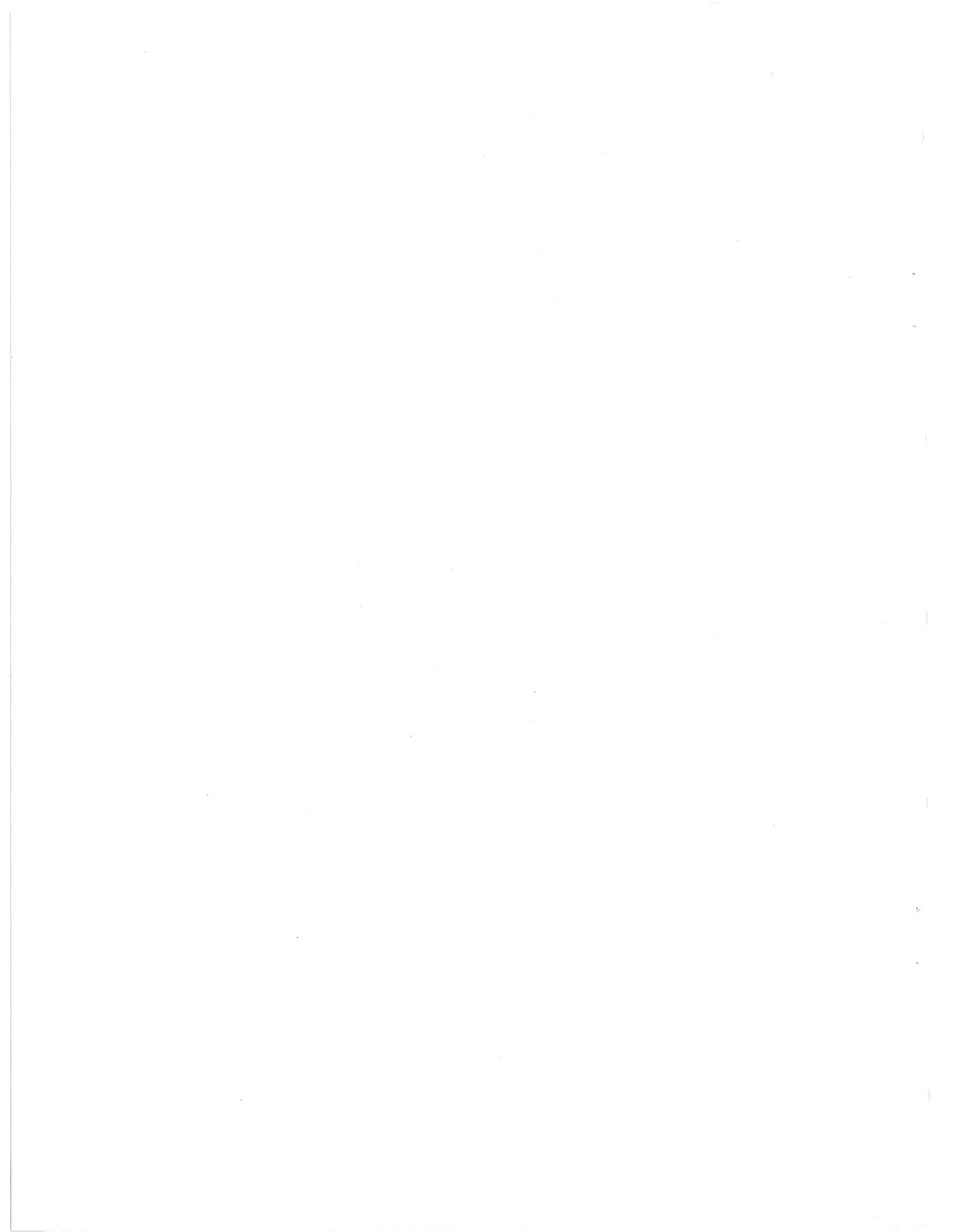
100 lb (approx).

**Operating Voltages DCL only:**

+5 Vdc

-15 Vdc

+15 Vdc



## CHAPTER 2

### PHYSICAL DESCRIPTION

The DCL itself is a 9-inch wide by 32-inch deep by 35-inch high unit that attaches at the left of the Drive assembly when the RP04 is viewed from the front (Figure 1-1). The DCL assembly is attached to the drive assembly by four 2-inch long  $1/4 \times 20$  bolts. The DCL assembly also has its own casters for easy roll-away when disconnected from the Drive assembly. Levelers are attached to provide stability when the DCL is permanently installed.

Physically, the DCL is comprised of three main subassemblies: The Card Nest and Cable Assembly, the Power Supply, and the Power Monitor (Figures 2-1 and 2-2).

#### **2.1 CARD NEST AND CABLE ASSEMBLY**

The card nest and cable assembly is accessible through the rear of the unit by lifting the entire rear cover panel and drawing it free of the assembly. This exposes the two fasteners that are used to hold the card nest and cable assembly (Figure 2-1) in an upright position. Then access to the printed circuit cards is gained by:

1. Loosening the two fastener screws and carefully swinging the assembly outward until it rests in a horizontal position.
2. Loosening the two fastener screws (Figure 2-2) on the air flow cover and swinging the cover to the vertical position. This exposes the hex and interface printed circuit boards (PCBs).

All control logic circuits are housed on the hex PCBs that extend the full length of the card nest and cable assembly. The PCBs that interface with the drive assembly and the two controllers are the smaller PCBs situated to the left of the assembly when viewed from the top. Figure 2-3 shows the layout of the PCBs within the card nest and cable assembly.

##### **2.1.1 Hex Printed Circuit Boards**

There are five hex PCBs. Designations for these cards are based on the principle control circuits housed on a particular PCB. For example, the Error Correction (EC) PCB is so designated because there are more ICs used for this function than for any other control function on this particular board. This does not mean, however, that other ICs on this same PCB are not used for control functions completely unrelated to error correction. The designations used are simply a convenient means of labeling and identifying the hex PCBs.

The hex PCBs are broken down as follows:

**RG (Registers) PCB:** This board contains most of the registers used to interface the DCL with the controller.

**DP (Dual Port or Dual Controller) PCB:** This card logic used to to implement DCL accessing by either of two controllers.

**SS (Seek and Search) PCB:** This board primarily includes the control logic to execute all mechanical operations.

**SN (Synchronous Transfer) PCB:** Much of the logic on this board implements synchronous data transfers between controller and disk pack.

**EC (Error Correction) PCB:** Approximately half of the logic on this PCB implements the error correction process. The remaining logic is used for error registers and timing.

### **2.1.2 MASSBUS and MDLI Interface PCBs**

Of the eight interface PCBs, six are used to convey signals between the DCL and MASSBUS A/MASSBUS B. Each of these six PCBs has two cable connectors (J1, J2) mounted directly on the card to accommodate the appropriate MASSBUS cables. Figure 2-3 shows the MASSBUS PCB locations and designations.

The two interface cards closest to the hex PCBs house the transceiver circuits for conveying signals between the DEC 733 Drive and the DCL. These PCBs are called the MDLI interface cards (Figure 2-3).

## **2.2 POWER SUPPLY**

The front of the DCL Assembly houses the H764 supply that develops operating voltages for the card nest and cable assembly. This unit is accessible from the front of the DCL assembly when the front panel is removed (Figure 2-4). Access to the voltage adjust potentiometers is via the metal hole plugs. The power supply components can be replaced by removing the four front panel screws (Figure 2-5).

The power supply attaches at its base to a mounting bracket located in the center of the DCL assembly. The top attaches to a bracket directly above the front panel.

## **2.3 POWER MONITOR**

The power monitor is situated beneath the power supply (Figure 2-4) and provides a constant check of the power supply output voltage conditions. When any voltage (line or dc output) strays from the required tolerance (ac low or dc low), this unit notifies the system. The power monitor also provides the "power OK" signal used to initialize the RP04 following power up. The power monitor attaches at the base of the DCL assembly with four mounting screws.

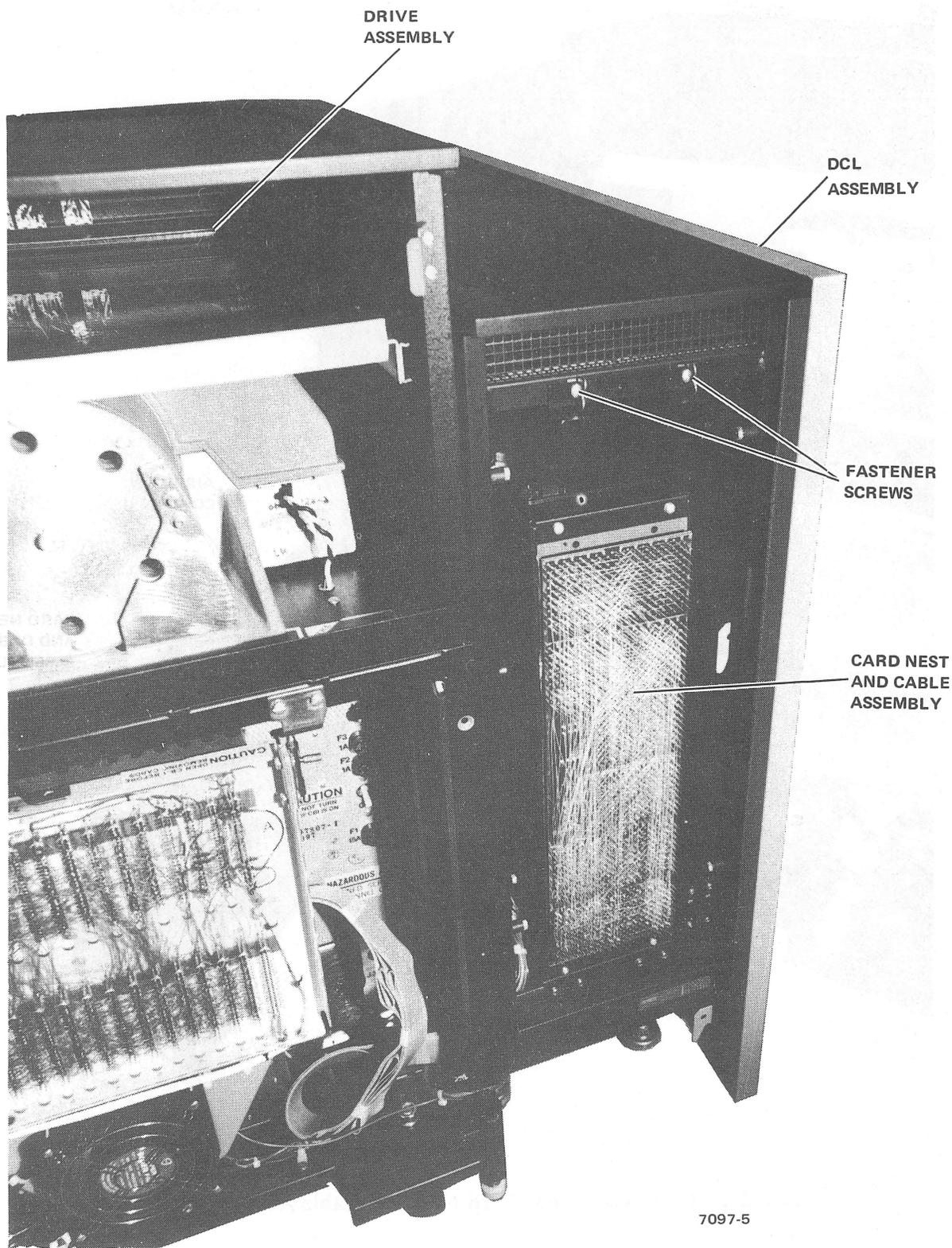


Figure 2-1 RP04 Drive and DCL Assemblies Back View, Rear Panels Removed

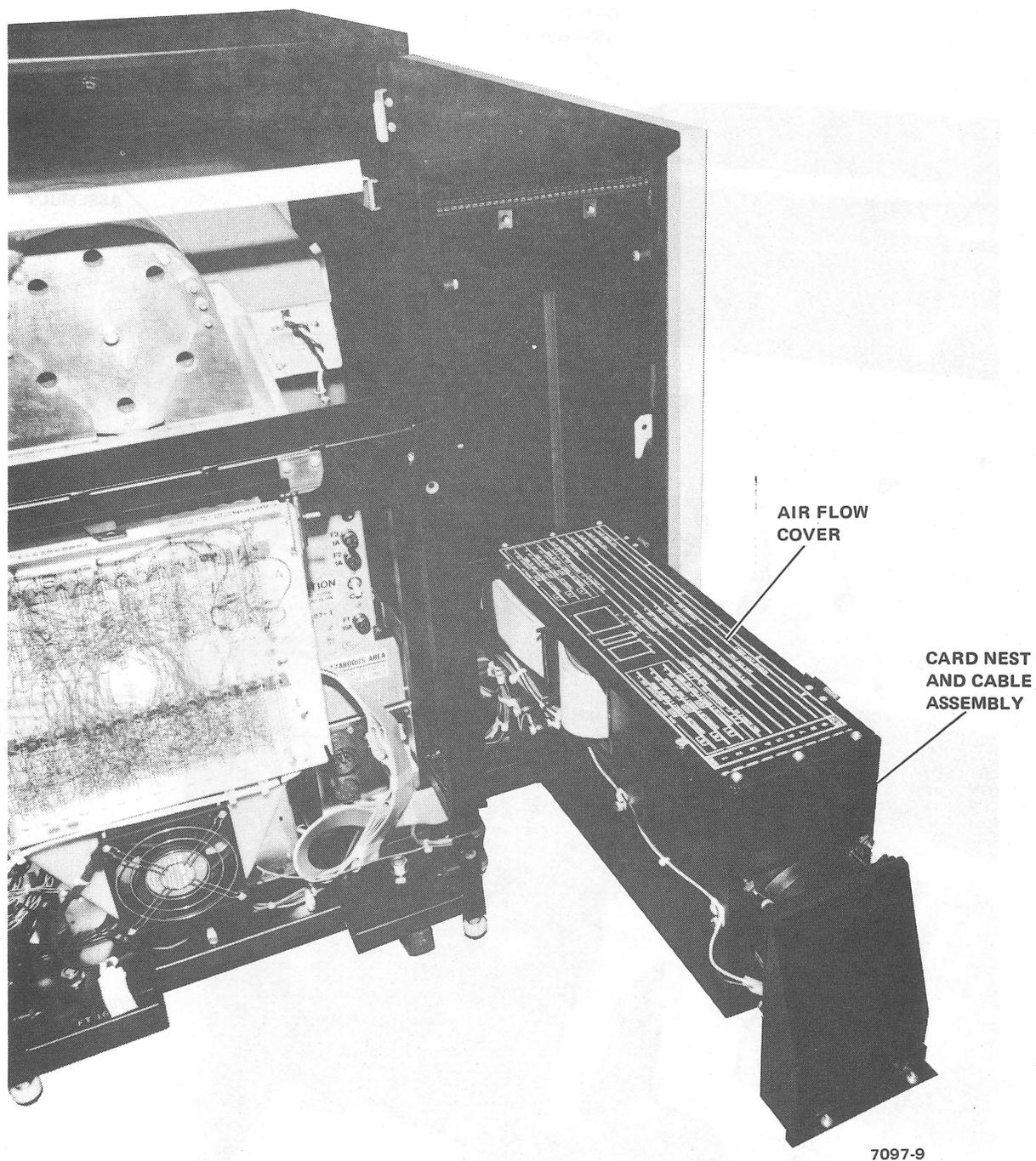


Figure 2-2 DCL Rear View, Card Nest and Cable Assembly Extended

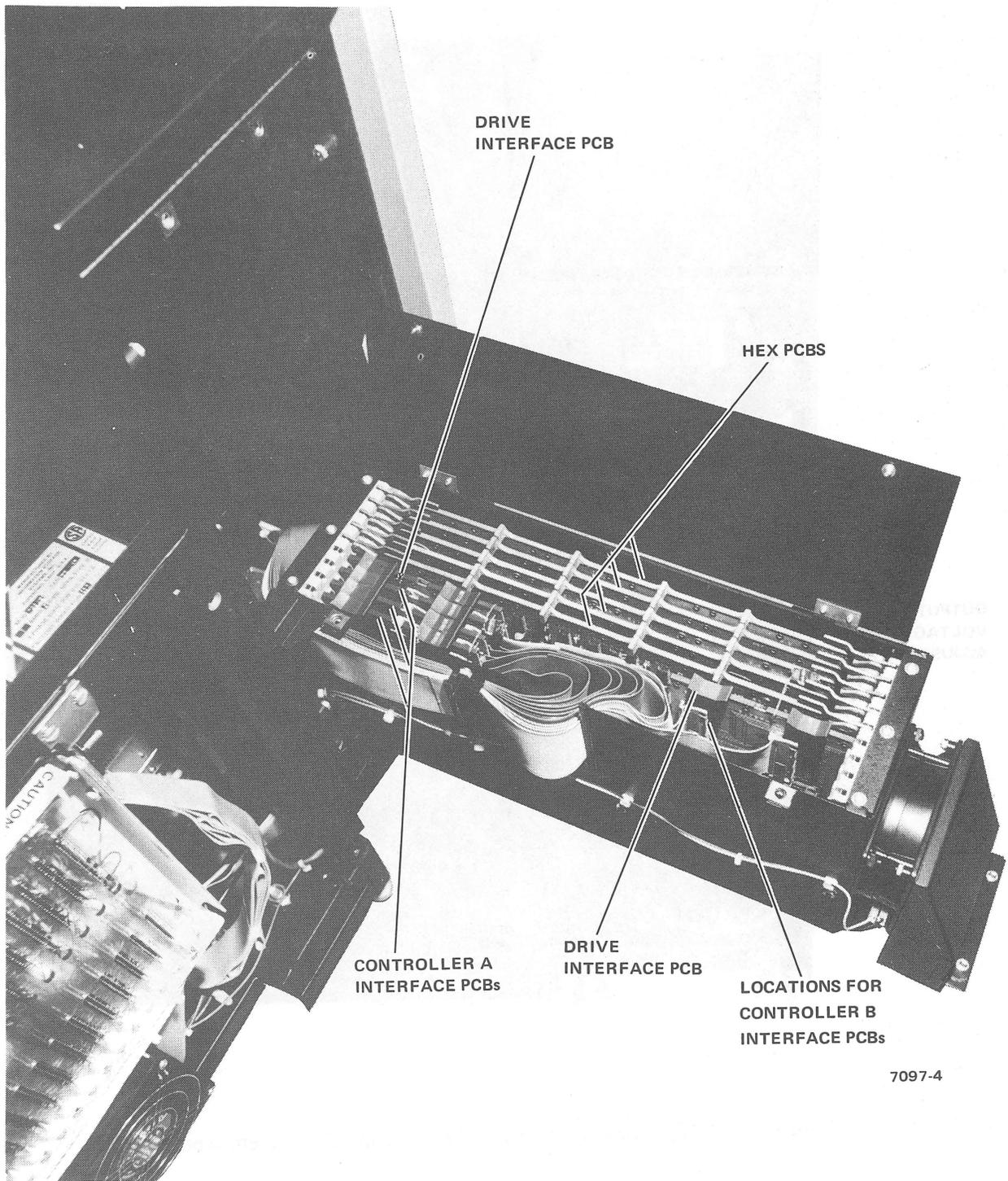
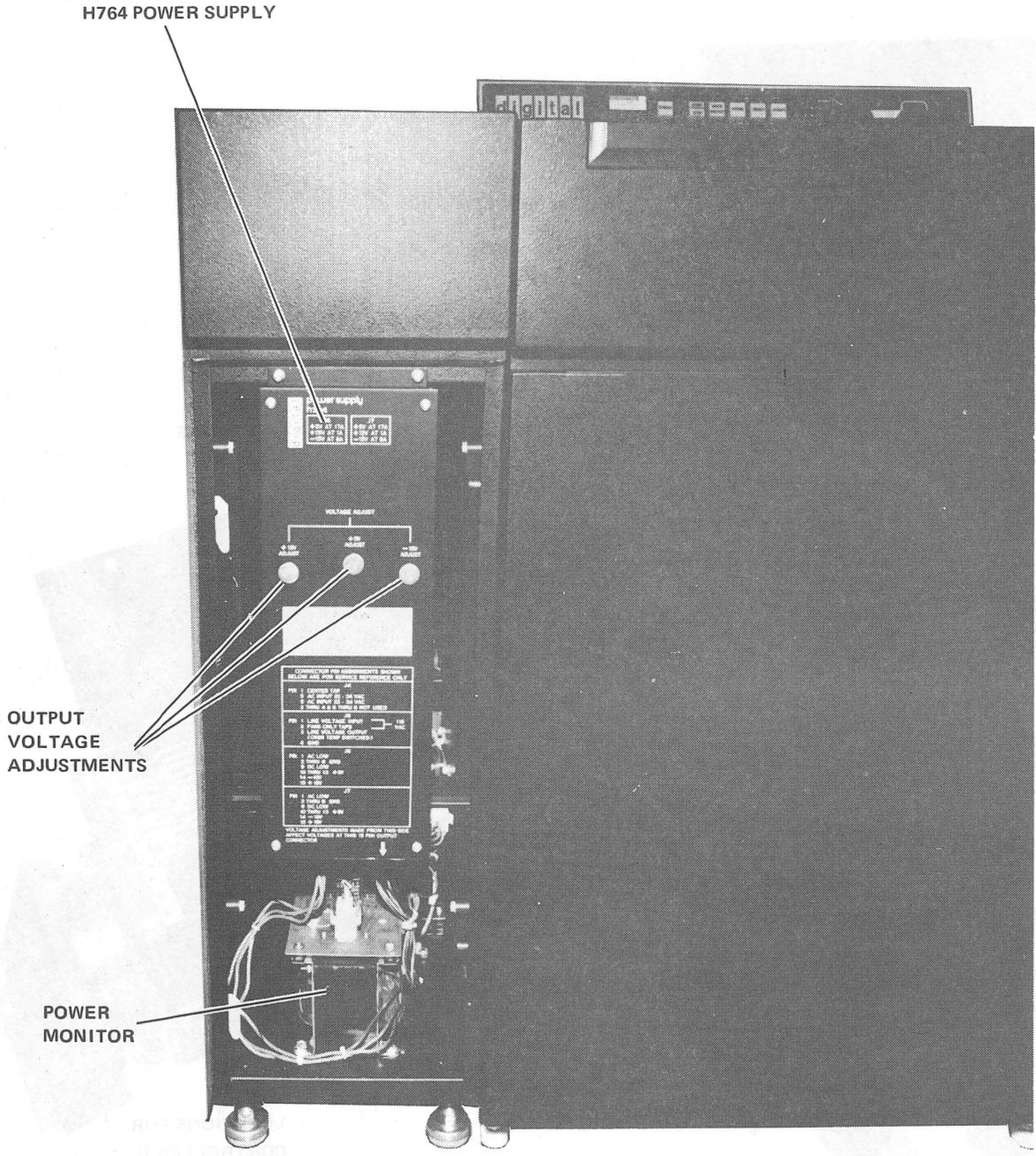
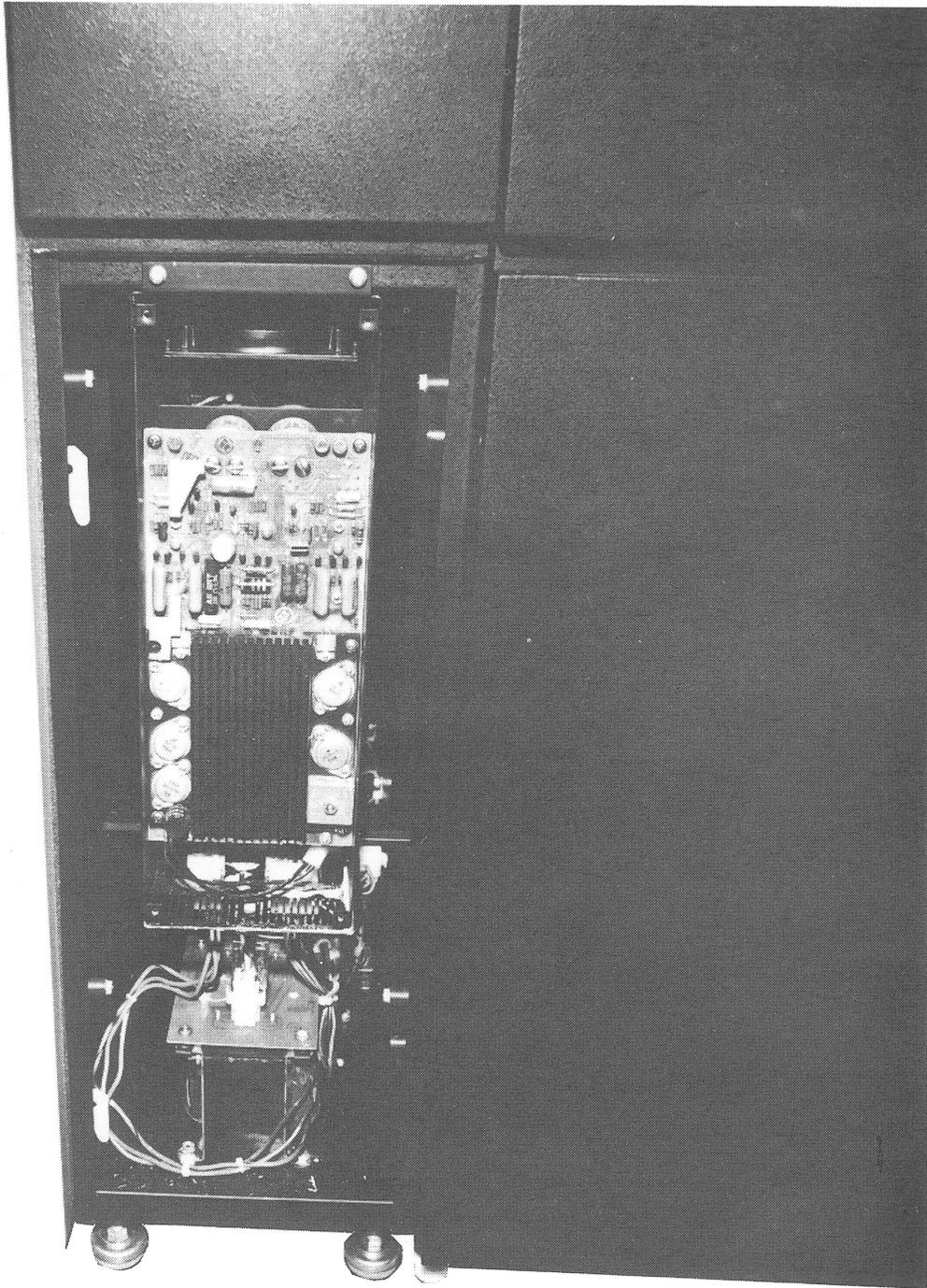


Figure 2-3 Card Nest and Cable Assembly PCB Layout



7097-3

Figure 2-4 DCL Assembly Front View, Front Panel Removed



7097-1

Figure 2-5 DCL Assembly Power Supply, Front Panel Removed



## CHAPTER 3

### DCL FUNCTIONAL DESCRIPTION

#### 3.1 DUAL CONTROLLER OPERATION

The DCL interface logic is designed to permit access by two different controllers (i.e., provided that the dual access option is installed). The setting of the CONTROLLER SELECT switch on the control panel determines whether a single or both controllers are allowed to access the RP04. When set to the A/B position, it allows for accessing by either controller on a "first-come, first-serve" basis. Once a controller has gained access in the dual access mode, it retains control until it has completed its operation. Normally, a controller releases the DCL by executing a release command to place the RP04 back in a device available status. However, if the accessing controller fails to execute such an instruction within a one-second time span (i.e., following the last operation), a timeout function produces the same result.

#### 3.2 READ/WRITE DATA TRANSFERS

Writing data words onto the RP04 disk pack or reading data words from the disk pack are termed synchronous data transfers since such transfers are effected over the synchronous data bus portion of the MASSBUS interface. Four read/write commands are implemented by the DCL logic. However, the write header and data command must first be used to format a disk pack (divide the disk surface into addressable sectors) as a prerequisite to executing the other three commands.

##### 3.2.1 Disk Pack Formatting

Each new disk pack must be formatted to provide each sector with an identifying indicator or label that defines sector number, track number, and cylinder number. This labeling information is inserted into what is called the header area of a sector, which can also contain additional identifying information (key field data) under program control. Because the header area is positioned before the data field of a sector, the header area information can be used to accurately address specific disk pack sectors for read/write operation.

To format a new disk pack, use the write header and data command. Prior to executing this command, the central processor writes the initial cylinder, track, and sector address information into the appropriate DCL registers. The central processor has the header information (cylinder, track, sector, and key field words) ready on the synchronous data lines so that when the command is executed and the addressed sector is found, the header information is present for writing onto the disk. The header information is supplied to the RP04 by the operating system.

Executing the write header and data command causes the DCL to initiate the process of finding the addressed cylinder, track, and sector. When all are found, the DCL informs the controller to send the header information. At this time, the DCL also initiates the sequence for serially writing each header word onto the disk surface. In this way, header information is introduced onto an addressed sector.

The write header and data command also allows for writing data words beginning at a fixed time following the header. The area where data words are written is called the data field.

### 3.2.2 Other Read/Write Commands

The DCL interprets and executes three other commands to effect read/write transfers. For each of these commands, the DCL makes proper identification of the header prior to initiating the transfer process. The technique for header identification is to compare the cylinder, sector, and track addresses of the header against those supplied prior to the read/write command initiation. Failure to detect a matchup in all three addresses results in the DCL setting a header compare error bit that is eventually sampled by the central processor.

A breakdown of the remaining read/write commands and their functions is given below:

**Write Data Command:** This command is used to write data words into the data field of an addressed sector. The DCL executes this command by first finding and identifying the addressed sector and then initiating the write transfer into the data field of that sector. The command can be used for an extended (multi-sector) write operation in that the DCL continues to write into the data fields of successive sectors for as long as the RUN line from the controller is asserted.

**Read Header and Data Command:** This command reads the header and data fields of an addressed sector and sends both to the central processor via the controller. Reading the header information may prove useful in analyzing faults after the DCL has indicated a header compare error on a particular sector. By reading the header information (cylinder, track and sector address) and comparing it against that supplied with the read header and data command, the CPU is able to determine exactly what header (format) information is in error.

**Read Command:** This command is used to read the data field of an addressed sector. As is the case with all read/write commands, the CPU must load the desired cylinder address and desired sector/track registers prior to executing the command. Once the addressed sector has been found, the DCL reads consecutive sectors for as long as the RUN line from the controller is asserted.

### 3.3 DISK ADDRESSING TECHNIQUES AND RELATED COMMANDS

The DCL executes two commands that are used solely to locate addressed areas of the disk pack – seek and search. The functions carried out by these commands are broken down as follows:

**Seek Command:** This causes the drive read/write heads to be positioned over the addressed cylinder. Cylinder and track information is supplied from the central processor prior to executing the command. When the heads are correctly positioned, the drive informs the DCL which in turn asserts the ATTENTION line to the controller.

Read/Write commands may also require positioning the read/write heads at the addressed cylinder. This activity is referred to as an “implied seek,” since the seek command is not used and the ATTENTION line is not asserted.

**Search Command:** The search command is used as a method of optimizing the pack revolution time. When the DCL detects the addressed sector, it asserts the ATTENTION line to the controller.

### 3.4 DCL INTERFACE REGISTER

The DCL has 16 interface registers that can be accessed by the controller; they fall into the following general categories:

**Control –** The control register receives the command (read, write, seek, etc.) codes from the controller. The DCL control logic samples the content of this register and initiates the appropriate execution sequence.

Status – The bits of this register supply the central processor with DCL and Drive status information.

Maintenance – The maintenance register is used by diagnostic programs to initiate various maintenance functions.

Error Information – Three registers are provided to indicate error status within both the DCL and the Drive.

Address Data – These are five registers that are associated with disk addressing:

- Desired Cylinder Address Register
- Current Cylinder Address Register
- Desired Sector/Track Register
- Offset Register, used to offset the disk read/write heads in fixed increments.
- Look Ahead Register, can be used to subdivide the data field of a sector.

System Housekeeping – There are two registers used for system housekeeping, i.e., a drive type register and serial number register.

Attention Summary Pseudo Register – This is a one bit register used to indicate that the RP04 requires the attention of the system. In one sense it can be considered an interrupt line.

Error Correction – There are two registers used to convey error correction information to the central processor.

### **3.5 ERROR CORRECTION CAPABILITY**

The DCL is equipped with error correction logic, which (provided it is not inhibited by the system) becomes operative whenever an error is detected during a read operation. Once activated, the error correction circuits proceed to locate the error in the sector data field where the error occurred. When this area is detected, the DCL makes available the following information to the operating system:

1. Error correction code burst pattern.
2. Position within the data field where the error occurred.

Given this information, the software can determine the exact bits in error and correct them.

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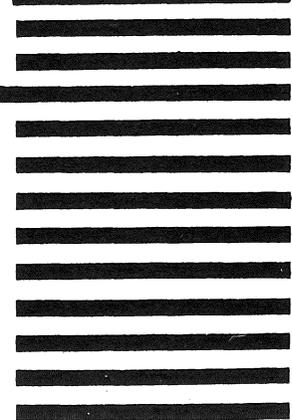
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