



NV430VX Motherboard Technical Product Specification

Order Number 281821-001

August 1996

The NV430VX motherboard may contain design defects or errors known as errata. Characterized errata that may cause the NV430VX motherboard's behavior to deviate from published specifications are documented in the NV430VX Motherboard Specification Update.



Revision History

Revision	Revision History	Date
001	First release of the NV430VX TPS	8/96

This product specification applies only to standard NV430VX motherboards with BIOS identifier 1.00.0x.DN0.

Changes to this specification will be published in the NV430VX Motherboard Specification Update (order number 281827) before being incorporated into a revision of this document.

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1 Motherboard Description

1.1 Overview

The NV430VX motherboard supports Pentium® microprocessors operating at 75, 90, 100, 120, 133, 150, 166, 180, and 200 MHz, as well as Intel MMX™ technology Pentium processors. The motherboard features:

- LPX form factor
- Socket 7 Pentium OverDrive® processor socket

Main Memory

- Four 72-pin SIMM† sockets
- Support for up to 128 MB of Extended Data Out (EDO) or fast page memory
- Support for non-parity and parity DRAM

Second Level Cache Memory

- 256 KB or 512 KB Pipeline Burst SRAM soldered to the motherboard

Chipset and PCI/IDE Interface

- Intel 82430VX PCIsset
- Integrated PCI bus mastering controller
- Two fast IDE interfaces
- Support for up to four IDE devices

I/O Features

- PC87306B Super I/O controller
- Integrates standard I/O functions: floppy drive interface, one multi-mode parallel port, one FIFO serial port, real-time clock, keyboard and mouse controller, IrDA†-compatible interface
- Support for two Universal Serial Bus (USB) interfaces

Expansion Slots

- Up to 3 ISA
- Up to 3 PCI

Audio Subsystem

- Crystal 4236 codec audio component
- Wavetable upgrade header

Graphics Subsystem

- S3† ViRGE graphics controller
- VESA† feature connector
- TV out
- Video capture

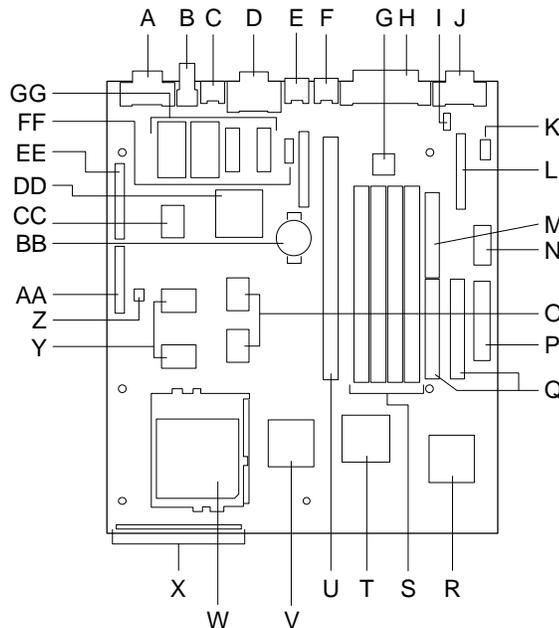
Other features

- Plug and Play compatible
- Support for Advanced Power Management

Software drivers and utilities are available from Intel.

1.2 Motherboard Manufacturing Options

- Crystal 4236 or 4237 audio CODEC
- 256 KB or 512 KB pipelined burst SRAM cache soldered to the board
- Support for universal serial bus (USB)
- S3 Trio64† V+ or ViRGE including EDO video memory
- Brooktree 829 video capture processor



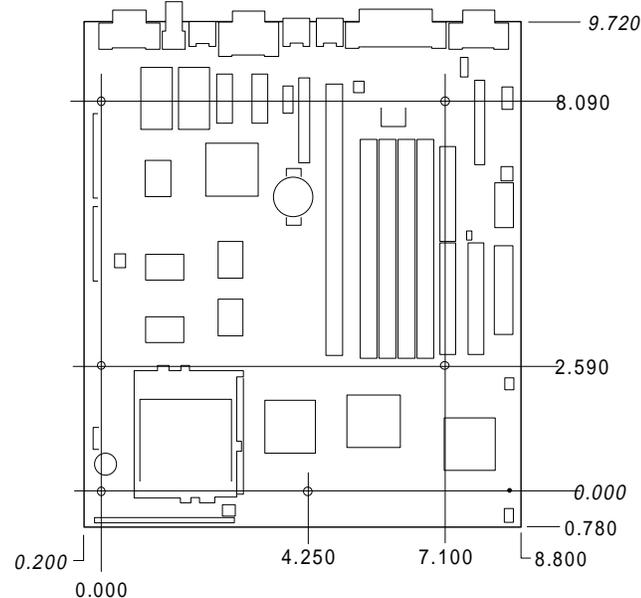
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Figure 1. Motherboard Features

- | | |
|---|--|
| A - VGA connector (Optional) | S - SIMM sockets |
| B - RCA video in connector (Optional) | T - 82371SB PCI ISA/IDE Accelerator (PIIX3) |
| C - I ² C I/O S-Video out connector (Optional) | U - Riser card connector |
| D - USB connector (Optional) | V - 82437VX (TVX) |
| E - PS/2† Keyboard port | W - Socket 7 Pentium Processor socket |
| F - PS/2 Mouse port | X - Front panel connectors |
| G - Crystal 4236 (Optional) | Y - 256K or 512K cache (Optional) |
| H - Parallel port connector | Z - PCI riser jumper |
| I - CD-ROM audio connector (Optional) | AA -Configuration jumper block |
| J - Serial port 2 connector | BB -Battery for real-time clock |
| K - Wavetable upgrade connector (Optional) | CC -Brooktree 829 video capture processor (Optional) |
| L - Audio I/O connector (Optional) | DD -S3 Trio64 V+ or ViRGE PCI graphics controller (Optional) |
| M - Floppy drive connector | EE -VESA/LPB connector (Optional) |
| N - 3.3V Power connector | FF - Serial port 1 connector |
| O - 82438VX (TDX) | GG -Graphics memory (Optional) |
| P - Primary Power connector | |
| Q - IDE connectors | |
| R - .National PC87306B I/O controller | |

1.3 Form Factor

The motherboard is designed to fit into a standard LPX form factor chassis. Figure 2 illustrates the mechanical form factor. The form factor adheres to the standard LPX guidelines in that the outer dimensions are 9 inches x 10.5 inches. Location of the I/O connectors, riser slot, and mounting holes are in strict compliance with the LPX specification.



OM04779

Figure 2. Board Dimensions

1.4 Microprocessor

The motherboard operates with 3.3 volt Pentium processors and 2.8 volt MMX technology Pentium processors. An onboard circuit detects the presence of a 3.3 volt or 2.8 volt processor. A linear voltage regulator circuit provides the required voltage from the 5.0 volt tap of the power supply. An on-board jumper enables use of VRE specified processors. Pentium processors that run internally at 75, 90, 100, 120, 133, 150, 166, 180, and 200 MHz are supported.

The Pentium processor maintains full backward compatibility with the 8086, 80286, Intel386™ and Intel486™ processors. The processor supports both read and write burst mode bus cycles. It also features separate 8 KB on-chip code and data write back caches.

The Pentium microprocessor is an advanced numeric coprocessor that maintains full backward compatibility with math coprocessors that comply with ANSI/IEEE standard 754-1985.

1.4.1 Microprocessor Upgrade

The motherboard provides a 321-pin Socket 7 ZIF processor socket. Socket 7 supports a processor upgrade path that includes higher performance Pentium OverDrive processors than can be supported with socket 5.

1.5 Memory

1.5.1 Main Memory

The motherboard has four SIMM sockets arranged in two banks: Bank 0 and Bank 1. Each bank has two sockets. SIMMs in the same bank must be the same type, size, and speed; SIMMs in different banks may differ in type, size, and speed. SIMMs must be installed in both sockets of a bank, and at least one bank must be filled. The BIOS automatically detects memory type and size so no jumper settings are required.

The motherboard supports:

- 72-pin SIMMs with tin-plated contacts
- 70 ns fast page mode SIMMs
- 60 or 70 ns extended data out (EDO) SIMMs; 70 ns parts are not supported for bus speed of 66 MHz
- Non-parity or parity SIMMs
- Single- or double-sided SIMMs in the following sizes:

SIMM size	Configuration (non-parity)	Configuration (parity)
4 MB	1 x 32	1 x 36
8 MB	2 x 32	2 x 36
16 MB	4 x 32	4 x 36
32 MB	8 x 32	8 x 36

1.5.1.1 EDO DRAM

EDO DRAM improves memory read performance by holding the memory data valid until the next CAS# falling edge unlike fast page mode DRAM, which tri-states the memory data when CAS# negates to precharge for the next memory cycle. With EDO DRAM, the CAS# precharge overlaps the data-valid time, which allows CAS# to negate earlier while still satisfying the memory data-valid window.

1.5.2 Second-Level Cache

Manufacturing options for second level (L2) cache are no cache, 256 KB, or 512 KB direct-mapped write-back cache. The L2 cache is contained in two global write enable (GWE) Pipeline Burst SRAM (PBSRAM) devices soldered to the motherboard. An 8 KB x 8 external Tag SRAM provides caching support for up to 64 MB of main memory. There are no upgrade options.

1.6 Chipset

The Intel 82430VX PCIsset consists of the 82437VX System Controller (TVX), two 82438VX Data Paths (TDX) and one 82371SB PCI/ISA IDE Xcelerator (PIIX3) bridge chip.

1.6.1 82437VX System Controller (TVX)

The 82437VX provides all control signals necessary to drive a second level cache and the DRAM array, including multiplexed address signals. The TVX also controls access to memory and generates snoop controls to maintain cache coherency. The TVX comes in a 208-pin QFP package and includes the following features:

- Microprocessor interface control
- Integrated L2 write-back cache controller
 - Pipeline burst SRAM
 - 256 or 512 KB direct-mapped
- Integrated DRAM controller
 - 64 bit path to memory
 - Support for EDO and fast page DRAM
 - 8 MB to 128 MB main memory
- Fully synchronous PCI bus interface
 - 25/30/33 MHz
 - PCI to DRAM > 100 Mbytes/sec
 - Up to 4 PCI masters in addition to the PIIX3 and IDE.

1.6.2 82438VX Data Path (TDX)

Two 82438VX data path components provide a 64-bit microprocessor to memory path. The TDX components are controlled by the TVX. They each add one load to the PCI bus and perform all of the required byte and word swapping. The TDX devices come in a 208 pin QFP package.

1.6.3 PCI/ISA IDE Xcelerator (PIIX3)

The PIIX3 provides the interface between the PCI and ISA buses and integrates a dual channel fast IDE interface capable of supporting up to 4 devices. The PIIX3 integrates seven 32-bit DMA channels, five 16-bit timer/counters, two eight-channel interrupt controllers, PCI-to-AT interrupt mapping circuitry, NMI logic, ISA refresh address generation, and PCI/ISA bus arbitration circuitry on to the same device. The PIIX3 comes in a 208-pin QFP package and includes the following features:

- Interface between the PCI and ISA buses
- Universal Serial Bus controller
 - Host/hub controller
- Integrated fast IDE interface
 - Support for up to 4 devices
 - PIO Mode 4 transfers up to 16 MB/sec
 - Integrated 8 x 32-bit buffer for bus master PCI IDE burst transfers
 - Bus master mode

- PCI 2.1 compliant
- Enhanced fast DMA controller
- Interrupt controller and steering
- Counters/timers
- SMI interrupt logic and timer with fast on/off mode

1.6.4 Universal Serial Bus (USB) Support

The motherboard provides two USB ports as a manufacturing option. This permits connection of two USB peripheral devices directly to the system without an external hub. If more devices are required, an external hub can be connected to either of the built-in ports. The motherboard completely supports the standard universal host controller interface (UHCI) and takes advantage of the standard software drivers written to be compatible with UHCI. Features of the USB include:

- Self-identifying peripherals
- Automatic mapping of function to driver and configuration
- Support for isochronous and asynchronous transfer types over the same set of wires
- Support for up to 127 physical devices
- Guaranteed bandwidth and low latencies appropriate for telephony, audio, and other applications
- Error handling and fault recovery mechanisms built into protocol
- Low cost cables and connectors. Low speed devices require shielded cables

1.6.5 IDE Support

The motherboard has two independent bus mastering PCI IDE interfaces that support PIO Mode 3, PIO Mode 4, and ATAPI (e.g., CD-ROM) devices. The BIOS supports Logical Block Addressing (LBA) and Extended Cylinder Head Sector (ECHS) translation modes. IDE device transfer rate and translation mode are automatically detected by the BIOS.

Normally, programmed I/O operations require a substantial amount of processor bandwidth; however, in true multi-tasking operating systems like Windows[†] 95, the bandwidth freed by bus mastering IDE can be devoted to other tasks while disk transfers are occurring.

1.7 Super I/O Controller

The PC87306B Super I/O Controller from National Semiconductor provides:

- Serial ports: two NS16C550-compatible UARTs with send/receive 16-byte FIFO
- Multimode bidirectional parallel port
 - Standard mode, IBM and Centronics compatible
 - Enhanced Parallel Port (EPP) mode with BIOS and driver support
 - High-speed Extended Capabilities Port (ECP) mode
- Industry standard floppy controller with 16-byte FIFO and 2.88 MB floppy drive support
- 8042-compatible keyboard controller

- Real-time clock accurate within +/- 13 minutes a year at 25°C and 5V
- Support for an IrDA-compliant infrared interface

By default, the I/O controller interfaces are automatically configured during boot up. The I/O controller can also be manually configured in the Setup program.

1.7.1 Serial Ports

The motherboard has one 9-pin D-Sub serial port connectors located on the back panel.

1.7.2 Parallel Port

The connector for the multimode bidirectional parallel port is a 25-pin D-Sub connector located on the back panel of the motherboard. In the Setup program, there are three options for parallel port operation:

- Compatible (standard mode)
- Bidirectional Enhanced Parallel Port (EPP). A driver from the peripheral manufacturer is required for operation.
- Bidirectional high-speed Extended Capabilities Port (ECP)

1.7.3 Floppy Controller

The I/O controller is software compatible with the DP8473 and 82077 floppy drive controllers. In the Setup program, the floppy interface can be configured for the following floppy drive capacities and sizes:

- 360 KB, 5.25-inch
- 1.2 MB, 5.25-inch
- 720 KB, 3.5-inch
- 1.2 MB, 3.5-inch (3 mode floppy driver required)
- 1.25/1.44 MB, 3.5-inch
- 2.88 MB, 3.5-inch

1.7.4 Keyboard and Mouse Interface

PS/2 keyboard and mouse connectors are located on the back panel of the motherboard. The 5 volt lines to these connectors are protected with a PolySwitch[†] circuit that, like a self-healing fuse, reestablishes the connection after an over-current condition is removed. While this device eliminates the possibility of having to replace a fuse, power to the computer should be turned off before connecting or disconnecting a keyboard or mouse.

⇒ **NOTE**

You can plug the mouse and keyboard into either connector.

The keyboard controller contains the AMI Megakey keyboard and mouse controller code, which provides the traditional keyboard and mouse control functions, and also supports Power On/Reset password protection. A Power On/Reset password can be specified in the Setup program.

The keyboard controller also supports the following hot-key sequences:

- <CTRL><ALT> Software reset. This key sequence resets the computer's software by jumping to the beginning of the BIOS code and running the Power On Self Test (POST).
- <CTRL><ALT><+> and <CTRL><ALT><-> Turbo mode. Note that Turbo mode could be affected by the operating system, or whether the processor is in protected mode or virtual x86 mode.
 - <CTRL><ALT><-> For Deturbo mode (emulates a 23 MHz AT)
 - <CTRL><ALT><+> For Turbo mode
- <CTRL><ALT><defined in Setup>: Power management. This key sequence invokes power managed mode, which reduces the computer's power consumption while maintaining its ability to service external interrupts.
- <CTRL><ALT><defined in Setup>: Keyboard lock. This key sequence is a security feature that locks the keyboard until the User password is entered. When keyboard lock is invoked, the keyboard LEDs flash. To enable the keyboard lock feature, a User password must be specified in the Setup program.

1.7.5 Real-Time Clock, CMOS RAM and Battery

The real-time clock is compatible with DS1287 and MC146818 components. It provides a time-of-day clock and a 100-year calendar with alarm features and century rollover. The real-time clock also supports 242-bytes of battery-backed CMOS RAM in two banks, which are reserved for BIOS use.

The time, date, and CMOS values can be specified in the Setup program. The CMOS values can be returned to their defaults by using the Setup program or by setting a configuration jumper on the motherboard.

An external coin-cell battery powers the real-time clock and CMOS memory. If the computer is not plugged into a wall socket, the battery has an estimated life of three years. When the computer is plugged in, the 5 volt standby current from the motherboard's power supply extends the life of the battery. The RTC is accurate to +/- 13 minutes/year at 25°C and 5V conditions.

1.7.6 Infrared Support

The motherboard has a 5-pin header that supports Hewlett Packard HSDSL-1000 compatible infrared (IR) transmitters/receivers. In the Setup program, Serial Port 2 can be directed to a connected IR device. The connection can be used to transfer files to or from portable devices like laptops, PDAs and printers. The Infrared Data Association (IrDA) specification supports data transfers of 115 Kbps at a distance of 1 meter.

1.7.6.1 Consumer Infrared Support

The motherboard has a signal pin that supports Consumer Infrared (IR) devices (remote controls). The signal pin supports receive only. Consumer IR devices can be used to control telephony functions and multimedia operations like volume and CD track changes. A software and hardware interface is needed to use this feature.

1.8 Graphics Subsystem

The NV430VX motherboard is available with a factory option of either an S3 Trio64 V+ or S3 ViRGE SVGA graphics. The NV430VX motherboard supports the S3 media channel, LPB, for HW MPEG.

1.8.1 S3 ViRGE Graphics

The factory option of an S3 ViRGE SVGA graphics controller with 2 MB of 50 ns EDO SOJ DRAM has a high performance 64-bit 2D/3D graphics engine. It incorporates the S3 Streams Processor[†] that enables the device to convert YUV formatted video data to RGB and provides acceleration for scaling the video display without compromising picture quality or frame rate. The on-chip RAMDAC/clock synthesizer is capable of output pixel data rates of 135 MHz providing non-interlaced screen resolutions of up to 1280x1024x256 colors at 75 Hz. The 64-bit S3d Engine incorporates the key Windows and other GUI accelerator functions of BitBLT, line draw and polygon fill. 3D features include flat shading, Gouraud shading and texture mapping support. Advanced texture mapping features include perspective correction, bi-linear and tri-linear filtering, MIP-mapping, and Z-buffering. These features provide the most realistic user experience for interactive 3D applications. In addition, a fast linear addressing scheme based upon DCI reduces software overhead by mapping the display memory into the microprocessor's upper memory address space and permitting direct microprocessor access to the display memory.

Table 1. S3 ViRGE Resolutions and Refresh Rates

2 MB Memory Resolution	Refresh Rate (Hz) at:				
	4-bit Color	8-bit Color	15/16-bit Color	24-bit Color	32-bit Color
640 x 480	60	60, 72, 75, 85	60, 72, 75	60, 72, 75*	60, 72, 75
800 x 600	not supported	56, 60, 72, 75, 85	60, 72, 75	60, 72, 75*	60, 72, 75
1024 x 768	not supported	43(IL), 60, 70, 75, 85	43(IL), 60, 70, 75	43(IL), 60, 70, 75*	not supported
1152 x 864	not supported	60	not supported	not supported	not supported
1280 x 1024	43(IL), 45(IL), 60, 72, 75*	45(IL), 60, 72, 75	not supported	not supported	not supported
1600 x 1200	not supported	48.5(IL)	not supported	not supported	not supported

* Non-accelerated mode only

IL Interlaced

1.8.2 S3 Trio64 V+ Graphics

The factory option of an S3 Trio64 V+ SVGA graphics controller with 1 MB of graphics DRAM is upgradeable to 2 MB. The graphics DRAM can be upgraded to 2 MB by installing two 256 KB x 16, 50 ns SOJ DRAM devices in the provided sockets. The Trio64 V+ has a 64-bit graphics engine and incorporates the S3 Streams Processor that enables the device to convert YUV formatted video data to RGB and provides acceleration for scaling the video display without compromising picture quality or frame rate. The on-chip RAMDAC/clock synthesizer is capable of output pixel data rates of 135 MHz providing non-interlaced screen resolutions of up to 1280x1024x256 colors at 75 Hz with 2 MB of DRAM. Hardware acceleration for graphics

functions such as BitBLTs with ROPs, 2-point line draws, trapezoidal and polygon fills, clipping and cursor support provide high performance operation under Windows and other GUI environments. In addition, a fast linear addressing scheme based upon DCI reduces software overhead by mapping the display memory into the microprocessor’s upper memory address space and permitting direct microprocessor access to the display memory.

Table 2. S3 Trio64 V+ Resolutions and Refresh Rates

1 MB Memory	Refresh Rate (Hz) at:				
Resolution	4-bit Color	8-bit Color	15/16-bit Color	24-bit Color	32-bit Color
640 x 480	60	60, 72, 75, 85	60, 72, 75	60, 72, 75*	not supported
800 x 600	not supported	56, 60, 72, 75, 85	60, 72, 75	60, 72, 75*	not supported
1024 x 768	not supported	43(IL), 60 ,70, 75, 85	not supported	not supported	not supported
1152 x 864	not supported	60	not supported	not supported	not supported
1280 x 1024	43(IL), 45(IL), 60, 72, 75*	not supported	not supported	not supported	not supported
1600 x 1200	not supported	not supported	not supported	not supported	not supported
2 MB Memory	Refresh Rate (Hz) at:				
Resolution	4-bit Color	8-bit Color	15/16-bit Color	24-bit Color	32-bit Color
640 x 480	60	60, 72, 75, 85	60, 72, 75	60, 72, 75*	60, 72, 75
800 x 600	not supported	56, 60, 72, 75, 85	60, 72, 75	60, 72, 75*	60, 72, 75
1024 x 768	not supported	43(IL), 60 ,70, 75, 85	43(IL), 60, 70, 75	43(IL), 60, 70, 75*	not supported
1152 x 864	not supported	60	not supported	not supported	not supported
1280 x 1024	43(IL), 45(IL), 60, 72, 75*	45(IL), 60, 72, 75	not supported	not supported	not supported
1600 x 1200	not supported	48.5(IL)	not supported	not supported	not supported

* Non-accelerated mode only

IL Interlaced

1.8.3 VESA/LPB Feature Connector

The NV430VX motherboard supports a 26-pin standard VESA feature connector for synchronizing graphics output with external devices like TV tuners and hardware MPEG. These devices share the frame buffer interface to maximize multimedia performance. They also share the LPB (Local Peripheral Bus), an 8-pin extension to the VESA connector, that provides a glueless bidirectional interface to a video companion device, such as an MPEG/live video decoder. The NV430VX also supports other VESA standards such as the VESA DPMS protocol to put a DPMS compliant monitor into power saving modes and the VESA Display Data Channel (DDC2B ver. 1) that permits transfer of monitor identification and resolution support data for ease of use.

1.8.4 Graphics Drivers and Utilities

Graphics drivers for OS/2[†] 2.11 and OS/2 WARP, MS-DOS[†] applications such as AutoCAD[†] and Microstation, as well as driver updates for Windows 3.11, Windows 95, Windows NT[†] may be downloaded from the Intel Applications Support BBS. Drivers for SCO[†] UNIX[†] are available from SCO.

1.8.5 Brooktree Video Capture

The NV430VX features an optional Brooktree Bt829 Video Capture Processor for TV/VCR applications. The Bt829 is a single-chip decoding and scaling solution for analog NTSC/PAL/SECAM input signals from TV tuners, VCR's, cameras, and other sources of composite or Y/C video. The NV430VX provides two inputs for video: an RCA input connector, and an S-Video input connector as part of a 7-pin mini-din connector on the motherboard I/O backpanel.

The Bt829 registers are accessed via a two-wire Inter-Integrated Circuit (I²C) interface provided on a 7-pin mini-din on the motherboard I/O backpanel.

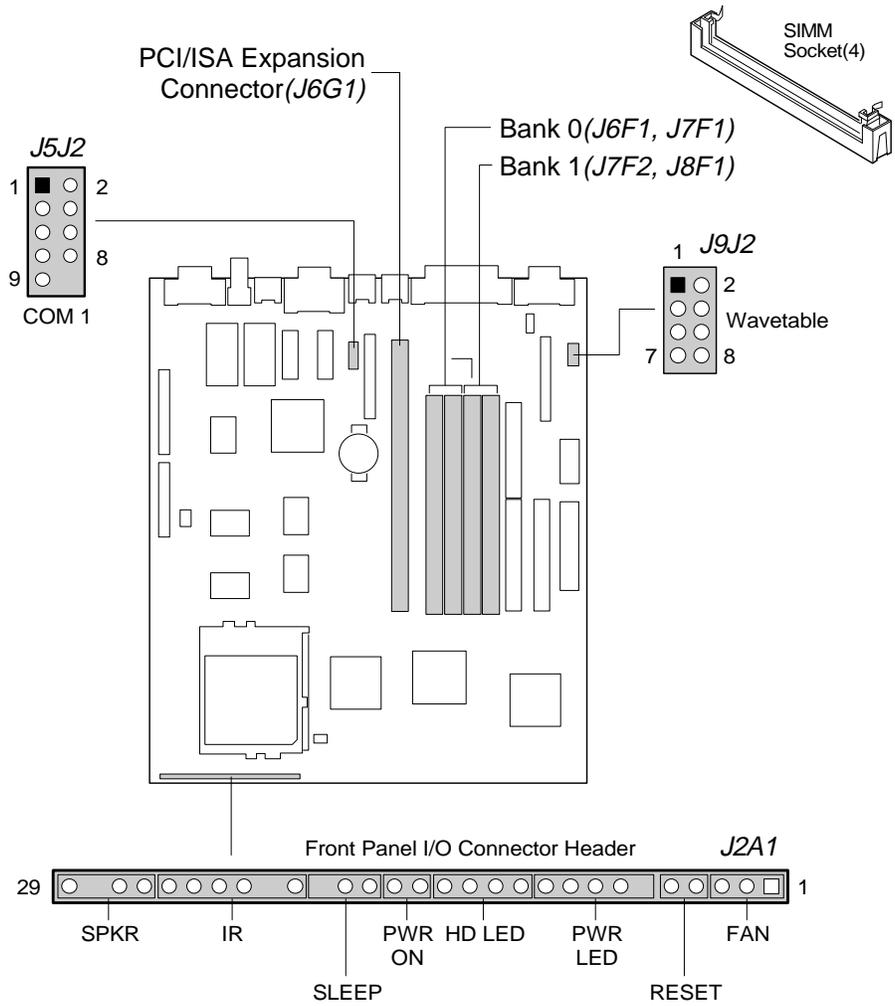
1.9 Audio Subsystem

1.9.1 Crystal CS4236

The CS4236 provides all the digital audio and analog mixing functions required for playing and recording of audio on personal computers. These functions include stereo analog-to-digital and digital-to-analog converters, analog mixing, anti-aliasing and reconstruction filters, line and microphone level inputs, and digital audio compression using selectable A-law / μ law, and full digital control of all mixer and volume control functions. With the integrated Sound Blaster[†] OPL3 compatible FM synthesizer, the CS4236 also provides support for four major sound standards including Adlib[†] and Sound Blaster Pro 2.0, Windows Sound System and MPU-401 to meet all of the requirements of today's multimedia applications. The CS4236 also supports full-duplex operation which ensures support for future applications such as video conferencing.

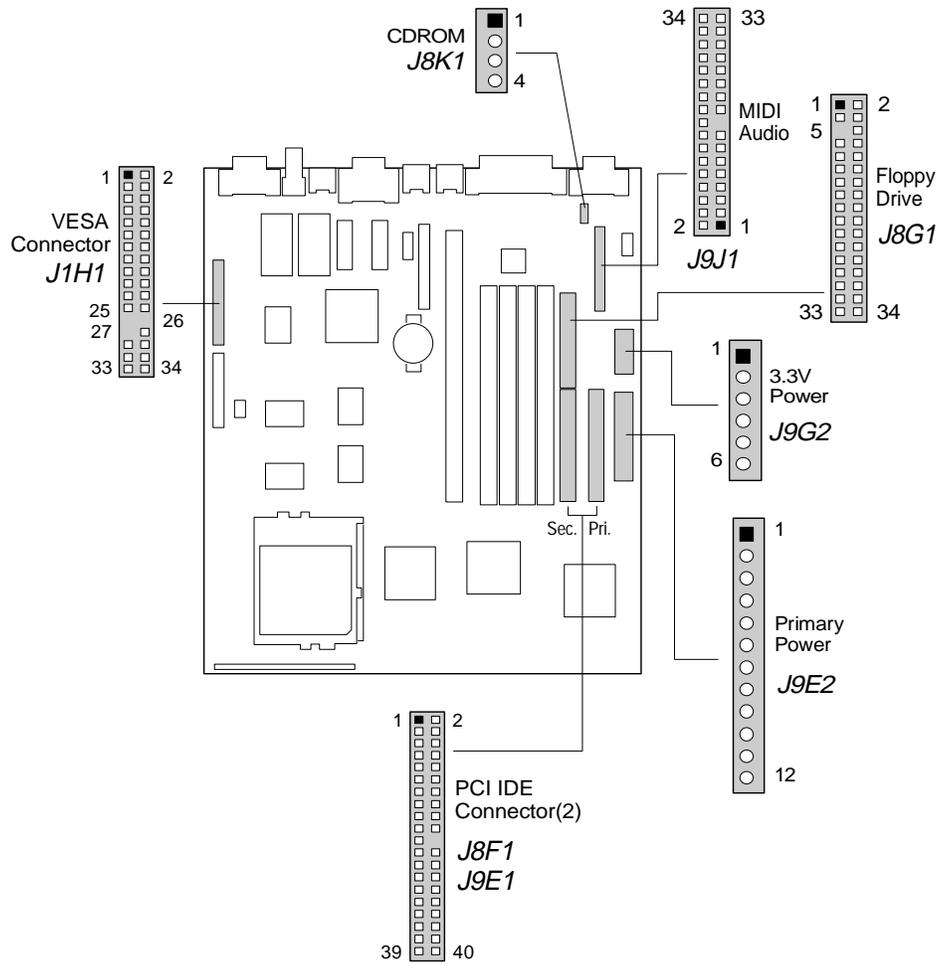
The CS4236 includes a full Plug and Play ISA interface and is comprised of seven logical devices including the Synthesizer, Game Port, Sound Blaster, Sound System, MPU-401, CD-ROM interface and the CS4236 device itself. Each logical device is configured into the host environment using the ISA Plug and Play configuration methodologies. The audio sub-system requires up to two DMA channels and one interrupt. The system can be configured to use either DMA channels 0, 1, or 3. The interrupt can be mapped to interrupt 5, 7, 9, 11, 12, or 15.

1.10 Motherboard Connectors



OM04775

Figure 3. Motherboard Connector Locations



OM04776

Figure 3. Motherboard Connector Locations (continued)

1.10.1 VESA Feature Connector - J1H1

Pin	Signal Name	Pin	Signal Name
1	Ground	2	Data 0
3	Ground	4	Data 1
5	Ground	6	Data 2
7	Video enable	8	Data 3
9	Sync enable	10	Data 4
11	PCLK enable	12	Data 5
13	N/C	14	Data 6
15	Ground	16	Data 7
17	Ground	18	PIX CLKR
19	Ground	20	BLANK
21	Ground	22	HSYNC
23	N/C	24	VSYNC
25	Key	26	Ground
27	Key	28	Key
29	Ground	30	IICCLK
31	NC	32	IICDAT
33	GOP1	34	ENFEAT

1.10.2 Serial 1 Connector - J5J2

Pin	Signal Name
1	DCD
2	DSR
3	Serial In# (SIN)
4	RTS
5	Serial Out# (SOUT)
6	CTS
7	DTR
8	RI
9	Ground
10	Key

1.10.3 CD Audio - J8K1

Pin	Signal Name
1	Ground
2	CD-Left
3	Ground
4	CD-Right

1.10.4 Wavetable Upgrade Connector - J9J2

Pin	Signal Name
1	Wave Right
2	Ground
3	Wave Left
4	Ground
5	Key
6	Ground
7	N/C
8	MIDI_OUT

1.10.5 MIDI/Audio Upgrade - J9J1

Pin	Signal Name	Pin	Signal Name
1	+5 V	2	+5 V
3	JoyStick But0	4	JoyStick But2
5	JoyStick X1	6	JoyStick X2
7	Ground	8	MIDI Out
9	Ground	10	JoyStick Y2
11	JoyStick Y1	12	JoyStick But3
13	JoyStick But1	14	MIDI In
15	+5 V	16	Mono Out
17	Key	18	Mono In
19	Line Out Right	20	Ground
21	Right Speaker	22	Ground
23	Left Speaker	24	Key
25	Line Out Left	26	Ground
27	Line In Right	28	-12 V
29	Line In Left	30	Ground
31	Mic In	32	+12 V
33	Ground	34	Ground

1.10.6 Floppy Drive Connector - J8G1

Pin	Signal Name	Pin	Signal Name
1	Ground	2	DENSEL
3	Ground	4	Reserved
5	Key	6	FDEDIN
7	Ground	8	Index#
9	Ground	10	Motor Enable A#
11	Ground	12	Drive Select B#
13	Ground	14	Drive Select A#
15	Ground	16	Motor Enable B#
17	MSEN1	18	DIR#
19	Ground	20	STEP#
21	Ground	22	Write Data#
23	Ground	24	Write Gate#
25	Ground	26	Track 00#
27	MSEN0	28	Write Protect#
29	Ground	30	Read Data#
31	Ground	32	Side 1 Select#
33	Ground	34	Diskette Change#

1.10.7 3.3 V Power Connector - J9G2

Pin	Name
1	Ground
2	Ground
3	Ground
4	+3.3 V
5	+3.3 V
6	+3.3 V

1.10.8 Primary Power Connector - J9E2

When used with a power supply that supports remote power on/off, the motherboard can turn off the power via software control (soft-off). The Powerman utility supplied for Windows 3.1x allows for soft-off as does the shutdown icon in the Windows 95 Start menu. The BIOS will turn the power off when it receives the proper APM command from the operating system. For example, Windows 95 will issue this APM command when the user selects “Shutdown the computer” option. Note that APM must be enabled in the BIOS and the operating system in order for the soft-off feature to work correctly.

Pin	Name
1	PWRGD
2	+5 V
3	+12 V
4	-12 V
5	Ground
6	Ground
7	Ground
8	Ground
9	-5 V
10	+5 V
11	+5 V
12	+5 V

1.10.9 IDE Connectors - J8F1, J9E1

Pin	Signal Name	Pin	Signal Name
1	Reset IDE	2	Ground
3	Host Data 7	4	Host Data 8
5	Host Data 6	6	Host Data 9
7	Host Data 5	8	Host Data 10
9	Host Data 4	10	Host Data 11
11	Host Data 3	12	Host Data 12
13	Host Data 2	14	Host Data 13
15	Host Data 1	16	Host Data 14
17	Host Data 0	18	Host Data 15
19	Ground	20	Key
21	DDRQ0 (DDRQ1)	22	Ground
23	I/O Write	24	Ground
25	I/O Read#	26	Ground
27	IOCHRDY	28	Vcc pull-up

continued 

IDE Connectors (continued)

Pin	Signal Name	Pin	Signal Name
29	DDACK0 (DDACK1)#	30	Ground
31	IRQ14 (IRQ15)	32	Reserved
33	Addr 1	34	Reserved
35	Addr 0	36	Addr 2
37	Chip Select 1P (1S)#	38	Chip Select 3P (3S)#
39	Activity#	40	Ground

1.10.10 PCI/ISA Riser Connector - J6G1

Pin	Signal Name	Pin	Signal Name	Pin	Signal	Pin	Signal Name
A1	IOCHK#	B1	GND	E1	GND	F1	GND
A2	SD7	B2	RSTDRV	E2	GND	F2	GND
A3	SD6	B3	Vcc	E3	PCIINT1#	F3	PCIINT3#
A4	SD5	B4	IRQ9	E4	PCIINT2#	F4	PCIINT4#
A5	SD4	B5	-5 V	E5	Vcc	F5	Vcc
A6	SD3	B6	DRQ2	E6	Key	F6	Key
A7	SD2	B7	-12 V	E7	Vcc	F7	Vcc
A8	SD1	B8	0WS#	E8	PCIRST#	F8	PCKLF
A9	SD0	B9	+12 V	E9	GNT0#	F9	GND
A10	IOCHRDY	B10	GND	E10	REQ0#	F10	GNT1#
A11	AEN	B11	SMEMW#	E11	GND	F11	GND
A12	SA19	B12	SMEMR#	E12	PCKLE	F12	REQ1#
A13	SA18	B13	IOW#	E13	GND	F13	AD31
A14	SA17	B14	IOR#	E14	AD30	F14	AD29
A15	SA16	B15	DACK3#	E15	3.3 V	F15	3.3 V
A16	SA15	B16	DRQ3	E16	Key	F16	Key
A17	SA14	B17	DACK1#	E17	3.3 V	F17	3.3 V
A18	SA13	B18	DRQ1	E18	AD28	F18	AD27
A19	SA12	B19	REFRESH#	E19	AD26	F19	AD25
A20	SA11	B20	SYSCLK	E20	AD24	F20	CBE3#
A21	SA10	B21	IRQ7	E21	AD22	F21	AD23
A22	SA9	B22	IRQ6	E22	AD20	F22	AD21
A23	SA8	B23	IRQ5	E23	AD18	F23	AD19
A24	SA7	B24	IRQ4	E24	3.3 V	F24	3.3 V
A25	SA6	B25	IRQ3	E25	Key	F25	Key
A26	SA5	B26	DACK2#	E26	3.3 V	F26	3.3 V

continued ➡

PCI/ISA Riser Connector (continued)

Pin	Signal Name	Pin	Signal Name	Pin	Signal	Pin	Signal Name
A27	SA4	B27	TC	E27	AD16	F27	AD17
A28	SA3	B28	BALE	E28	FRAME#	F28	IRDY#
A29	SA2	B29	Vcc	E29	CBE2#	F29	DEVSEL#
A30	SA1	B30	OSC	E30	TRDY#	F30	PLOCK#
A31	SA0	B31	GND	E31	STOP#	F31	PERR#
C1	SBHE#	D1	MEMCS16#	G1	SDONE	H1	SERR#
C2	LA23	D2	IOCS16#	G2	SBO#	H2	AD15
C3	LA22	D3	IRQ10	G3	CBE1#	H3	AD14
C4	LA21	D4	IRQ11	G4	PAR	H4	AD12
C5	LA20	D5	IRQ12	G5	GND	H5	GND
C6	LA19	D6	IRQ15	G6	Key	H6	Key
C7	LA18	D7	IRQ14	G7	GND	H7	GND
C8	LA17	D8	DACK0#	G8	AD13	H8	AD10
C9	MEMR#	D9	DRQ0	G9	AD11	H9	AD8
C10	MEMW#	D10	DACK5#	G10	AD9	H10	AD7
C11	SD8	D11	DRQ5	G11	CBE0#	H11	AD5
C12	SD9	D12	DACK6#	G12	AD6	H12	AD3
C13	SD10	D13	DRQ6	G13	AD4	H13	AD1
C14	SD11	D14	DACK7#	G14	AD2	H14	AD0
C15	SD12	D15	DRQ7	G15	Key	H15	Key
C16	SD13	D16	Vcc	G16	Vcc	H16	Vcc
C17	SD14	D17	MASTER#	G17	GNT2	H17	Vcc
C18	SD15	D18	GND	G18	GND/REQ2*	H18	GND/PCCLK2*
				G19	GND	H19	GND

* These signals are 2-slot/3-slot jumpered signal names

1.10.11 Front Panel Connector - J2A1

Pin	Signal Name
1	Fan Neg
2	Fan Pos
3	Fan Neg
4	Ground
5	RESET
6	Key
7	PWRPU
8	PWRPU
9	Ground
10	Ground
11	HDD-PU
12	HDA
13	PWRDRV
14	PWRPU
15	SW_ON
16	Ground
17	SLEEP
18	SLEEPPU
19	Key
20	Vcc
21	NC
22	IRDA
23	Ground
24	IRTX
25	CONIRRRX
26	SPKROUT
27	SPKSRC
28	Key
29	Ground

1.10.12 Front panel Connectors

The board provides header connectors to support functions typically located on the chassis bezel. Front panel features supported include:

- Speaker
- Infrared (IrDA) port
- Sleep/resume
- Power on switch
- Hard drive activity LED
- Power LED
- Reset
- Fan

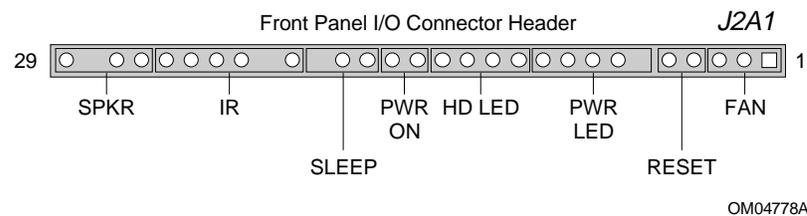


Figure 4. Front Panel I/O Connectors

1.10.12.1 Speaker

The external speaker provides error beep code information during the Power-On Self Test, if the BIOS cannot use the video interface. If there are no speakers plugged into the audio output jack, the audio output is redirected to the external speaker.

1.10.12.2 Infrared

Serial port 2 can be configured to support an IrDA or Consumer Ir module via a front panel header connector. Once configured for IrDA, the user can transfer files to or from portable devices such as laptops, PDA's, and printers using application software such as LapLink[†]. The IrDA specification provides for data transfers at 115 Kbps from a distance of 1 meter. Consumer Ir is typically used for remote control of telephony and multimedia functions.

1.10.12.3 Sleep/Resume

When Advanced Power Management (APM) is activated in the BIOS and the Operating System's APM driver is loaded, Sleep mode (Stand-By) can be entered in one of three ways: an optional front panel "Sleep/Resume" button, a user defined keyboard hot key, or prolonged inactivity. The Sleep/Resume button is supported by a 2-pin header located on the front panel I/O connector. Closing the "Sleep" switch will generate an SMI (System Management Interrupt) to the processor which immediately goes into System Management Mode (SMM), the so called "Sleep" mode.

The front panel "Sleep mode" switch must be a momentary two pin SPST type that is normally open. The function of the Sleep/Resume button can also be achieved via a keyboard hot-key sequence, or by a time-out of the inactivity timer. Both the keyboard hot-key and the inactivity

timer are programmable in Setup (timer is set to 10 minutes by default). To re-activate the computer, or “Resume”, the user must simply press the sleep/resume button again, or use the keyboard or mouse. Mouse activity will only “wake up” the computer if a mouse driver is loaded. While the computer is in Stand-By or “sleep” mode it is fully capable of responding to and servicing external interrupts (such as incoming FAX) even though the monitor will only turn on if a user interrupt (keyboard/mouse) occurs as mentioned above.

1.10.12.4 Power On Switch

The system’s front panel ON/OFF button is connected to the motherboard via the 1x4-pin “PS SLEEP” header (J2A1). Pins 15 and 16 of this connector should be tied to a SPST momentary button to support a power button and, likewise, pins 17 and 18 provide support for a energy saving sleep/resume button. These functions can be integrated into a computer as two separate buttons or a single button. By implementing a DPST momentary button connected to all four pins of the PS SLEEP connector, both sleep/resume and power on/off functions can be supported via a single button. In this configuration, pressing the button momentarily (closing the switch) while the computer is off will turn the computer on as you would expect (POST is run). Pressing the button while the computer is running (computer will beep), causes the computer to enter the energy saving Stand By (sleep) mode. Pressing the button (or keyboard/mouse) while the computer is sleeping, causes the computer to resume to full power and return to whatever application was active before entering sleep mode. To turn the computer off using the front panel button, the button must be pressed (computer will beep) and held down (2 seconds) until the computer produces a two-toned beep. At that time the computer will power off. Remember, the computer may also be powered off by utilizing the soft-off feature mentioned above. When the button is pressed again, the computer will power on and run POST. Traditional power supplies with mechanical ON/OFF buttons (those that do not support soft-off) will bypass these connectors.

1.10.12.5 Hard Drive Activity LED

This header can be connected to an LED to provide a visual indicator for when an IDE hard drive connected to the onboard IDE controller is being read or written.

1.10.12.6 Power LED

This header can be connected to an LED to provide a visual indicator for when the motherboard is powered on.

1.10.12.7 Reset

This header can be connected to a momentary SPST type switch that is normally open. When the switch is closed, the computer will hard reset and run POST.

1.10.12.8 Fan

This header can be connected to an auxiliary fan for additional cooling in the computer.

1.10.13 Back Panel Connectors

The back panel provides external access to PS/2 style keyboard and mouse connectors as well as one serial and one parallel port, which are integrated on the motherboard.

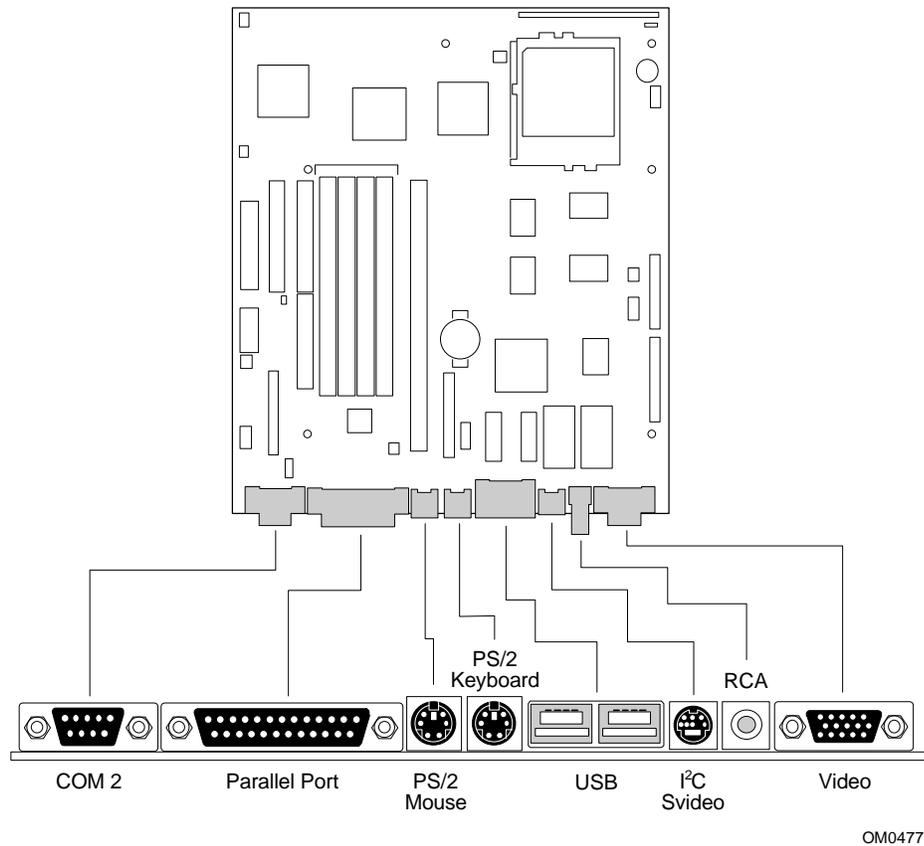


Figure 5. I/O Connections

1.10.13.1 PS/2 Keyboard Connector

Pin	Signal Name
1	Data
2	Mouse Data
3	Ground
4	+5 V (fused)
5	Clock
6	Mouse Clock

1.10.13.2 PS/2 Mouse Connector

Pin	Signal Name
1	Data
2	+5 V (main)
3	Ground
4	+5 V (standby)
5	Clock
6	No connect

1.10.13.3 Serial Port 2 Connector

Pin	Signal Name
1	DCD
2	Serial In#
3	Serial Out#
4	DTR#
5	GND
6	DSR#
7	RTS#
8	CTS#
9	GND

1.10.13.4 RCA Connector

Pin	Signal Name
1	Ground
2	COMPIN

1.10.13.5 I²C/S Video Out Connector

Pin	Signal Name
1	Ground
2	Ground
3	YIN
4	CIN
5	IICCLK
6	+12 V
7	IICDAT

1.10.13.6 Parallel Port Connector

Pin	Signal Name	Pin	Signal Name
1	Strobe#	14	Auto Feed#
2	Data bit 0	15	Fault#
3	Data bit 1	16	INIT#
4	Data bit 2	17	SLCT IN#
5	Data bit 3	18	Ground
6	Data bit 4	19	Ground
7	Data bit 5	20	Ground
8	Data bit 6	21	Ground
9	Data bit 7	22	Ground
10	ACK#	23	Ground
11	Busy	24	Ground
12	Error	25	Ground
13	Select		

1.10.13.7 Video Monitor Connector - J1J1

Pin	Signal Name
1	Red
2	Green
3	Blue
4	No connect
5	Ground
6	Ground
7	Ground
8	Ground
9	No connect
10	Ground
11	No connect
12	No connect
13	Horizontal Sync
14	Vertical Sync
15	No connect

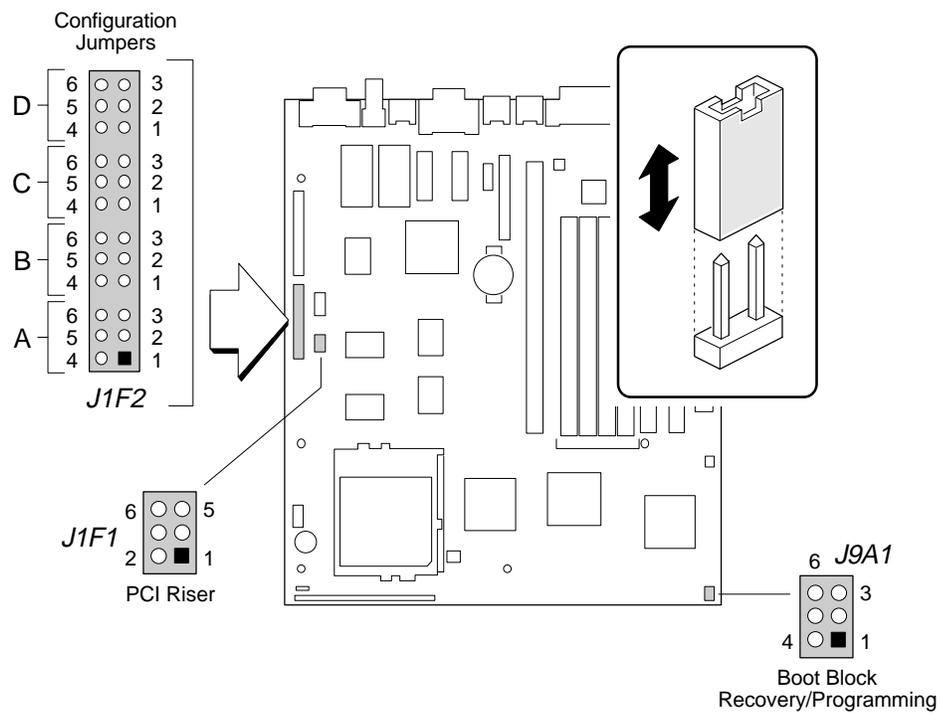
1.10.13.8 USB Connector 1

Pin	Signal Name
1	Vcc
2	USBP0#
3	USBP0
4	Ground

1.10.13.9 USB Connector 2

Pin	Signal Name
5	Vcc
6	USBP1#
7	USBP1
8	Ground

1.11 Jumper Settings



OM04777

Figure 6. Jumper Locations

Table 3. Configuration Jumper Settings

Function	Jumper	Configuration
Host Bus Speed (Note: These jumpers also set PCI and ISA clock speeds.)	J1F2-C	See Table 4
Microprocessor Speed Ratio	J1F2-D	See Table 4
CMOS Clear	J1F2-A	4-5 Keep (Default) 5-6 Clear
Password Clear	J1F2-A	1-2 Password Enabled (Default) 2-3 Password Clear/Disabled
Setup Access	J1F2-B	1-2 Access Allowed (Default) 2-3 Access Denied
Processor voltage	J1F2-B	4-5 Standard voltage (Default) 5-6 VRE enabled
PCI Riser	J1F1	1-2, 4-5 Two PCI slots on the riser card (Default) 2-3, 5-6 Three PCI slots on the riser card
BIOS Recovery	J9A1	1-2 Normal Operation (Default) 2-3 Recovery Mode
Boot Block Programming	J9A1	4-5 Normal Operation (Default) 5-6 Program Mode

1.11.1 Microprocessor Configuration - J1F2 C, D

These allow the motherboard to be switched between different speeds of the Pentium processor. These jumpers also affect the PCI and ISA clock speeds according to the following table.

Table 4. Microprocessor/Bus Speed Settings

Microprocessor Freq. (MHz)	Host Bus Freq. (MHz)	C	D	Microprocessor Clock Multiplier
200	66	1-2,5-6	1-2,5-6	3
180	60	2-3, 4-5	1-2, 5-6	3
166	66	1-2,5-6	2-3,5-6	2.5
150	60	2-3,4-5	2-3,5-6	2.5
133	66	1-2,5-6	2-3,4-5	2
120	60	2-3,4-5	2-3,4-5	2
100	66	1-2,5-6	1-2,4-5	1.5
90	60	2-3,4-5	1-2,4-5	1.5
75	50	2-3,5-6	1-2,4-5	1.5
reserved	-	2-3,5-6	1-2,5-6	
reserved	-	2-3,4-5	1-2,5-6	

1.11.2 Clear CMOS - J1F2 A

Allows CMOS settings to be reset to default values by moving the jumper from pins 4-5 to pins 5-6 and turning the computer on. When the BIOS reports that “NVRAM cleared by jumper”, the computer can be turned off, and the jumper should be returned to the 4-5 position to restore normal operation. This procedure should be done whenever the BIOS is updated. Default is for this jumper to be on pins 4-5.

1.11.3 Password Clear - J1F2 A

Allows the user password to be cleared by moving the jumper from pins 1-2 to pins 2-3 and turning the computer on. The computer should then be turned off and the jumper should be returned to the 1-2 position to restore normal operation. This procedure should only be done if the user password has been forgotten. The password function is effectively disabled if this jumper is in the 2-3 position. Default is for the password to be enabled (1-2 position).

1.11.4 Setup Access - J1F2 B

Allows access to Setup to be disabled by moving this jumper from the 1-2 position to the 2-3 position. Default is for access to Setup to be enabled (1-2 position).

1.11.5 CPU Voltage - J1F2-B

This jumper block changes the output of the on-board voltage regulator. Pins 4-5 should be jumpered for processors that require standard voltage regulation. Pins 5-6 should be jumpered for processors that require the VRE specification. This jumper should not be changed by the user unless changing to a new processor type. Some upgrade processors may require a different setting. Check the processor's documentation for the correct setting. (Standard = 3.135-3.63V, VR = 3.3-3.465V, VRE = 3.465-3.63V)

1.11.6 PCI Riser - J1F1

Allows routing of an extra IRQ and ID select to the riser card for an additional PCI slot to support a maximum of 3 PCI slots on a riser. Default is set for 2 PCI slots on the riser card (1-2 and 4-5 positions).

1.11.7 Program Boot Block Enable - J9A1

This jumper allows the boot block to be programmed when set to Program (pins 5-6). The default setting is for normal operation (pins 4-5).



CAUTION

Changing this jumper and reprogramming the boot block could cause unreliable operation.

1.11.8 BIOS Recovery - J9A1

This jumper allows the BIOS to be recovered, if it has been corrupted, by moving the jumper from the 1-2 position to the 2-3 position and inserting a recovery diskette. Default setting is for normal operation (1-2 position).

1.12 Environmental

Table 5. Motherboard Environmental Specifications

Parameter	Specification															
Temperature																
Non-Operating	-40°C to +70°C															
Operating	+0°C to +55°C															
DC Voltage																
+5 V	±5 %															
-5 V	±5 %															
+12 V	±5 %															
-12 V	±5 %															
+3.3 V	±5 %															
Shock																
Unpackaged	50 G trapezoidal waveform Velocity change of 170 inches/second															
Packaged	Half sine 2 millisecond															
	<table border="1"> <thead> <tr> <th>Product (Weight)</th> <th>Free fall (height in inches)</th> <th>Velocity (Change - inches/second)</th> </tr> </thead> <tbody> <tr> <td><20 lbs</td> <td>36</td> <td>167</td> </tr> <tr> <td>21-40 lbs</td> <td>30</td> <td>152</td> </tr> <tr> <td>41-80 lbs</td> <td>24</td> <td>136</td> </tr> <tr> <td>81-100 lbs</td> <td>18</td> <td>118</td> </tr> </tbody> </table>	Product (Weight)	Free fall (height in inches)	Velocity (Change - inches/second)	<20 lbs	36	167	21-40 lbs	30	152	41-80 lbs	24	136	81-100 lbs	18	118
Product (Weight)	Free fall (height in inches)	Velocity (Change - inches/second)														
<20 lbs	36	167														
21-40 lbs	30	152														
41-80 lbs	24	136														
81-100 lbs	18	118														
Vibration																
Unpackaged	5 Hz to 20 Hz : 0.01g ² Hz sloping up to 0.02 g ² Hz 20 Hz to 500 Hz : 0.02g ² Hz (flat)															
Packaged	10 Hz to 40 Hz : 0.015g ² Hz (flat) 40 Hz to 500 Hz : 0.015g ² Hz sloping down to 0.00015 g ² Hz															

1.13 Regulatory Compliance

This printed circuit assembly meets the following safety and EMI regulations when correctly installed in a compatible host computer.

1.13.1 Safety

1.13.1.1 UL 1950 - CSA 950-95, 3rd edition, 28 July 1995

The Standard for Safety of Information Technology Equipment including Electrical Business Equipment. (USA and Canada)

1.13.1.2 CSA C22.2 No. 950-93, 2nd Edition

The Standard for Safety of Information Technology Equipment including Electrical Business Equipment. (Canada)

1.13.1.3 EN 60 950, 2nd Edition, 1992 (with Amendments 1, 2, and 3)

The Standard for Safety of Information Technology Equipment including Electrical Business Equipment. (European Union)

1.13.1.4 IEC 950, 2nd edition, 1991 (with Amendments 1, 2, and 3)

The Standard for Safety of Information Technology Equipment including Electrical Business Equipment. (International)

1.13.1.5 EMKO-TSE (74-SEC) 207/94

Summary of Nordic deviations to EN 60 950. (Norway, Sweden, Denmark, and Finland)

1.13.2 Electromagnetic Interference (EMI)

1.13.2.1 FCC Class B

Title 47 of the Code of Federal Regulations, Parts 2 and 15, Subpart B, pertaining to unintentional radiators. (USA)

1.13.2.2 CISPR 22, 2nd Edition, 1993

Limits and methods of measurement of Radio Interference Characteristics of Information Technology Equipment. (International)

1.13.2.3 EN 55 022, 1995

Limits and methods of measurement of Radio Interference Characteristics of Information Technology Equipment. (Europe)

1.13.2.4 EN 50 082-1, 1992

Generic Immunity Standard. Currently compliance is determined via testing to IEC 801-2, -3 and -4. (Europe)

1.13.2.5 VCCI Class 2 (ITE)

Implementation Regulations for Voluntary Control of Radio Interference by Data Processing Equipment and Electronic Office Machines. (Japan)

1.13.2.6 ICES-003, Issue 2

Interference-Causing Equipment Standard, Digital Apparatus. (Canada)

1.13.3 Product Certification Markings

This printed circuit assembly has the following product certification markings:

- European CE Mark
 - Marking on the board or shipping container.
- UL Recognition Mark
 - Marking is the UL File No. E139761 on the component side of the board and the PB No. on the solder side of the board. Board material flammability is 94V-1 or -0.
- Canadian Compliance Mark
 - Marking is a small c followed by a stylized backward UR on the component side of the board.

2 Motherboard Resources

2.1 Memory Map

Table 6. Memory Map

Address Range (Decimal)	Address Range (hex)	Size	Description
1024K-131072K	100000-8000000	127 M	Extended Memory
960K-1023K	F0000-FFFFF	64 K	AMI BIOS
952K-959K	EE000-EFFFF	8 K	Main BIOS (available as UMB)
948K-951K	ED000-EDFFF	4 K	ESCD (Plug and Play configuration area)
944K-947K	EC000-ECFFF	4 K	OEM logo (available as UMB)
896K-943K	E0000-EBFFF	48 K	BIOS reserved
800-895K	C8000-DFFFF	96 K	Available high DOS memory (open to ISA and PCI bus)
640K-799K	A0000-C7FFF	160 K	Off-board video memory and BIOS
639K	9FC00-9FFFF	1 K	Extended BIOS Data (moveable by QEMM [†] , 386MAX [†])
512K-638K	80000-9FBFF	127 K	Extended conventional
0K-511K	00000-7FFFF	512 K	Conventional

2.2 I/O Map

Table 7. I/O Map

Address (hex)	Size	Description
0000 - 000F	16 bytes	PIIX3 - DMA 1
0020 - 0021	2 bytes	PIIX3 - Interrupt Controller 1
002E - 002F	2 bytes	Ultra I/O Configuration
0040 - 0043	4 bytes	PIIX3 - Timer 1
0060	1 byte	Keyboard Controller Byte - Reset IRQ
0061	1 byte	PIIX3 - NMI, speaker control
0064	1 byte	Keyboard Controller, CMD/STAT Byte
0070, bit 7	1 bit	PIIX3 - Enable NMI
0070, bits 6:0	7 bits	PIIX3 - real-time clock, address
0071	1 byte	PIIX3 - real-time clock, data
0078	1 byte	Reserved - Board Configuration
0079	1 byte	Reserved - Board Configuration

continued 

Table 7. I/O Map (continued)

Address (hex)	Size	Description
0080 - 008F	16 bytes	PIIX3 - DMA Page Register
00A0 - 00A1	2 bytes	PIIX3 - Interrupt Controller 2
00B2	1 byte	APM control port
00B3	1 byte	APM status port
00C0 - 00DE	31 bytes	PIIX3 - DMA 2
00F0	1 byte	Reset Numeric Error
0170 - 0177	8 bytes	Secondary IDE Channel
01F0 - 01F7	8 bytes	Primary IDE Channel
0200 - 0207	8 bytes	Gameport Joystick
0220 - 022F	16 bytes	Sound Blaster / OPL3-SA base port
0270 - 0273	4 bytes	I/O read port for Plug and Play
0278 - 027B	4 bytes	Parallel Port 2
02E8 - 02EF	8 bytes	Serial Port 4
02F8 - 02FF	8 bytes	On-Board Serial Port 2
0330 - 0331	2 bytes	Audio - MPU-401
0376	1 byte	Sec IDE Channel Command Port
0377	1 byte	Sec IDE Channel Status Port
0378 - 037F	8 bytes	Parallel Port 1
0388 - 038B	4 bytes	Audio - FM Synth
03B0 - 03BB	4 bytes	S3 ViRGE
03BC - 03BF	4 bytes	Parallel Port 3
03C0 - 03DF	16 bytes	S3 ViRGE
03E8 - 03EF	8 bytes	Serial Port 3
03F0 - 03F5	6 bytes	Floppy Channel 1
03F6	1 byte	Primary IDE Channel Command Port
03F7 (Write)	1 byte	Floppy Channel 1 Command
03F7, bit 7	1 bit	Floppy Disk Change Channel 1
03F7, bits 6:0	7 bits	Primary IDE Channel Status Port
03F8 - 03FF	8 bytes	On-Board Serial Port 1
04D0 - 04D1	2 bytes	Edge/level triggered
LPT + 400h	8 bytes	ECP port, LPT + 400h
0530 - 0537	8 bytes	Windows Sound System base port
0608 - 060B	4 bytes	Audio - WSS
0CF8 - 0CFB*	4 bytes	PCI Configuration Address Reg.
0CF9	1 byte	Turbo & Reset Control Reg.
0CFC - 0CFF	4 bytes	PCI Configuration Data Register
FF00 - FF07	8 bytes	IDE Bus Master Reg.
FFA0 - FFA7	8 bytes	Primary Bus Master IDE Registers
FFA8 - FFAF	8 bytes	Secondary Bus Master IDE Registers

* Only by DWORD accesses.

2.2.1 Port 79 Definition

Bit	Description	Bit = 1	Bit = 0
0	Reserved	N/A	N/A
1	Soft Off capable power supply present	No	Yes
2	Onboard Audio present	Yes	No
3	External microprocessor clock	See Table 4	See Table 4
4	External microprocessor clock	See Table 4	See Table 4
5	Setup Disable	Enable access	Disable access
6	Clear CMOS	Keep values	Clear values
7	Password Clear	Keep password	Clear password

2.3 Soft-Off Control

The board design supports Soft-off control via the SMM code in the BIOS. This feature is a manufacturing option. The CS1 pinout of the I/O controller is connected to the Soft-off control line in the power supply circuit. The registers in the I/O controller that set the I/O address and control of the CS1 pin are NOT setup until the SMM code is activated. The code performs the following operations:

OUT 0Ch to I/O port 2Eh

OUT 75h to I/O port 2Fh

OUT 11h to I/O port 2Eh

OUT 00h to I/O port 2Fh

OUT 0Dh to I/O port 2Eh

OUT A0h to I/O port 2Fh

After setting the above registers, any read operation to I/O location 75h will trigger the Soft-off circuit and turn the power supply off.

2.4 PCI Configuration Space Map

Table 8. PCI Configuration Space Map

Bus Number (hex)	Dev Number (hex)	Function Number (hex)	Description
00	00	00	Intel 82439HX (TXC)
00	07	00	Intel 82371FB (PIIX3) PCI/ISA bridge
00	07	01	Intel 82371FB (PIIX3) IDE Bus Master
00	07	02	Intel 82371FB (PIIX3) USB
00	08	00	S3 Video Controller
00	0B	00	Optional PCI Expansion Slot (three slot riser card)
00	11	00	PCI Expansion Slot
00	13	00	PCI Expansion Slot

2.5 DMA Channels

Table 9. DMA Channels

DMA	Data Width	Resource
0	8- or 16-bits	Audio
1	8- or 16-bits	Audio
2	8- or 16-bits	Floppy
3	8- or 16-bits	Parallel Port
4		Reserved - Cascade channel
5	16-bits	Open
6	16-bits	Open
7	16-bits	Open

2.6 Interrupts

Table 10. Interrupts

IRQ	Resource
NMI	I/O Channel Check
0	Reserved, Interval Timer
1	Reserved, Keyboard buffer full
2	Reserved, Cascade interrupt from slave PIC
3	COM2*
4	COM1*
5	Audio*
6	Floppy
7	LPT1*
8	Real-time Clock
9	User available
10	USB*
11	WSS*
12	Onboard Mouse Port
13	Reserved, Math coprocessor
14	Primary IDE if present, else user available
15	Secondary IDE if present, else user available

* Typical interrupt assignment

3 Motherboard BIOS and Setup Program

3.1 Introduction

The board uses an Intel BIOS, which is stored in Flash EEPROM and upgraded using a floppy disk-based program. In addition to the Intel BIOS, the Flash EEPROM also contains the Setup program, Power-On Self Tests (POST), APM 1.1, the PCI auto-configuration utility, and Windows 95 ready Plug and Play. This board also supports BIOS shadowing, allowing the BIOS to execute from 64-bit on-board write-protected DRAM.

The BIOS displays a sign-on message during POST identifying the type of BIOS and a five-digit revision code. The initial production BIOS in the board will be identified as 1.00.0x.DN0.

Information on BIOS functions can be found in the IBM PS/2 and Personal Computer BIOS Technical Reference published by IBM, and the ISA and EISA Hi-Flex AMIBIOS Technical Reference published by AMI. Both manuals are available at most technical bookstores.

3.2 BIOS Flash Memory Organization

The Intel PA28FB002BX 2 Mb Flash component is organized as 256K x 8 (256 KB). The Flash device is divided into seven areas, as described in Table 11.

Table 11. Flash Memory Organization

System Address		FLASH Memory Area
FFFF0000H	FFFFFFFFH	64 KB Main BIOS
FFFE0000H	FFFEFFFFH	16 KB Boot block (Not FLASH erasable)
FFFEA000H	FFFEBFFFH	8 KB ESCD Area (Plug-N-Play data storage area)
FFFE9000H	FFFE9FFFH	4 KB Reserved for BIOS
FFFE8000H	FFFE8FFFH	4 KB OEM Logo Area
FFFE0000H	FFFE7FFFH	32 KB Reserved for BIOS
FFFD0000H	FFFDFFFFH	64 KB Reserved for BIOS
FFFC0000H	FFFCFFFFH	64 KB Reserved for BIOS

3.3 BIOS Upgrades

Flash memory makes distributing BIOS upgrades easy. A new version of the BIOS can be installed from a diskette. BIOS upgrades are available to be down loaded from Intel's FTP site ([ftp.intel.com/pub/bios/](ftp://ftp.intel.com/pub/bios/)).

The disk-based Flash upgrade utility, FMUP.EXE, has three options for BIOS upgrades:

- The Flash BIOS can be updated from a file on a disk;
- The current BIOS code can be copied from the Flash EEPROM to a disk file as a backup in the event that an upgrade cannot be successfully completed; or
- The BIOS in the Flash device can be compared with a file to ensure the motherboard has the correct version.

The upgrade utility ensures the upgrade BIOS extension matches the target motherboard to prevent accidentally installing a BIOS for a different type of motherboard.

3.4 PCI IDE Support

The two local bus IDE connectors with independent I/O channel support are setup up automatically by the BIOS if the user selects “Autoconfiguration” in Setup. The IDE interface supports PIO Mode 3, and Mode 4 hard drives and recognition of ATAPI CD-ROMs, tape drives, and any other ATAPI devices. The BIOS will determine the capabilities of each drive and configure them to optimize capacity and performance. For the high capacity hard drives typically available today, the drive will be automatically be configured for Logical Block Addressing (LBA) for maximum capacity and to PIO Mode 3 or 4 depending on the capability of the drive. Mixing IDE drives, on the same cable, that offer different transfer modes is supported. Each drive’s mode is supported independently. The user is able to override the auto-configuration options by using the manual mode setting.

3.5 PCI Auto-configuration

The PCI auto-configuration utility operates in conjunction with the Setup program to allow the insertion and removal of PCI cards to the computer without user intervention (Plug and Play). When the computer is turned on after adding a PCI add-in card, the BIOS automatically configures interrupts, I/O space, and other parameters. PCI interrupts are distributed to available ISA interrupts that have been not been assigned to an ISA card or other resource. Those interrupts left set to “available” in Setup will be considered free for PCI add-in card use. It is nondeterministic as to which PCI interrupt will be assigned to which ISA IRQ.

The PCI Auto-Configuration function complies with version 2.10 of the PCI BIOS specification. Computer configuration information is stored in ESCD format. The ESCD data may be cleared by setting the CMOS clear jumper to the ON position.

PCI specification 2.1 for add-in card auto-configuration is also a part of the Plug and Play BIOS. Peer-to-peer hierarchical PCI Bridge 1.0 is supported, and by using an OEM supplied option ROM or TSR, a PCI-to-PCMCIA bridge capability is possible as well.

3.6 ISA Plug and Play

The BIOS incorporates ISA Plug and Play capabilities as delivered by Plug and Play Release 1.0A (Plug and Play BIOS V.. 1.0A, ESCD V.. 1.03). When used in conjunction with the ISA Configuration Utility (ICU) for DOS or Windows 3.x, the BIOS allows auto-configuration of Plug and Play ISA cards, PCI cards, and resource management for legacy ISA cards. Because the BIOS

supports configuring devices across PCI bridges, release 1.41 or greater of the ICU must be used with the board to properly view and change settings. Configuration information is stored in ESCD format. The ESCD data may be cleared by setting the CMOS clear jumper to the ON position.

The BIOS also has a Setup option to support the Windows 95 run time plug and play utilities. When this option is selected, only devices critical to booting are assigned resources by the BIOS. Device Node information is available for all devices to ensure compatibility with Windows 95.

Copies of the IAL Plug and Play specification may be obtained via the Intel WWW site at <http://www.intel.com>.

3.7 Advanced Power Management

The BIOS has support for Advanced Power Management (APM version 1.1). The energy saving Stand By mode can be initiated by a keyboard hot key sequence set by the user, a time-out period set by the user, or by a suspend/resume button tied to the front panel sleep connector.

When in Stand-by mode, the board reduces power consumption by utilizing the Pentium processor's System Management Mode (SMM) capabilities and also spinning down hard drives and turning off VESA DPMS compliant monitors. The user may select which DPMS mode (Stand By, Suspend, or Off) send to the monitor in Setup. The ability to respond to external interrupts is fully maintained while in Stand-by mode allowing the computer to service requests such as incoming FAX's or network messages while unattended. Any keyboard or mouse activity brings the computer out of the energy saving Stand By mode. When this occurs the monitor and IDE drives are turned back on immediately.

APM is enabled in BIOS by default, however, the computer must be configured with an APM driver in order for the power saving features to take effect. Windows 95 will enable APM automatically upon detecting the presence of the APM BIOS.

3.8 Language Support

The Setup screen and help messages are supported in 32 languages. There are 5 languages translated at this time for use: American English, German, Italian, French, and Spanish. Translations of other languages will available at a later date.

With a 1 Mb Flash BIOS, only one language can be resident at a time. The default language is American English, and will always be present unless another language is programmed into the BIOS using the Flash Memory Update Program (FMUP) available on the Intel BBS.

3.9 Boot Options

Booting from CD-ROM is supported in adherence to the “El Torito” bootable CD-ROM format specification developed by Phoenix Technologies and IBM. Under the *Boot Options* field in Setup, *CD-ROM* is one of four possible boot devices which are defined in priority order. The default setting is for floppy to be the primary boot device and hard drive to be the secondary boot device. If CD-ROM is selected, it must be the first device. The third and fourth devices are set to *disabled* in the default configuration. The user can also select *network* as a boot device. The network option allows booting from a network add-in card with a remote boot ROM installed.

⇒ NOTE

A copy of “El Torito” is available on the Phoenix Web page (<http://www.ptltd.com/techs/specs.html>).

3.10 Flash Logo Area

The motherboard supports a 4 KB programmable Flash user area located at EC000-ECFFF. An OEM may use this area to display a custom logo. The BIOS accesses the user area just after completing POST. A utility is available from Intel to assist with installing a logo into flash for display during POST. Contact your local Intel Sales office or authorized distributor for further information.

3.11 Setup Enable Jumper

A motherboard configuration jumper controls access to the Setup program. By setting the jumper to the disable position, the user is prevented from accessing the Setup program during the Power-On Self Test or at any other time. The message prompting the user to press <F1> to enter Setup is also disabled.

3.12 Setup Program

The ROM-based Setup program allows the configuration to be modified without opening the computer for most basic changes. The Setup program is accessible only during the Power-On Self Test (POST) by pressing the <F1> key after the POST memory test has begun and before boot begins. A prompt may be enabled that informs users to press the <F1> key to access Setup. A jumper setting on the motherboard can be set to prevent user access to Setup for security purposes.

3.12.1 Overview of the Setup Menu Screens

The Setup program initially displays the Main menu screen. In each screen there are options for modifying the BIOS configuration. Select a menu screen by pressing the left <←> or right <→> arrow keys. Use the up <↑> or down <↓> arrow keys to select items in a screen. Use the <Enter> key to select an item for modification. For certain items, pressing <Enter> will bring up a subscreen. After you have selected an item, use the arrow keys to modify the setting.

Table 12. Overview of the Setup Menu Screens

Setup Menu Screen	Description
Main	For setting up and modifying some of the basic options of a PC, such as time, date, diskette drives, hard drives.
Advanced	For modifying the more advanced features of a PC, such as peripheral configuration and advanced chipset configuration.
Security	For specifying passwords that can be used to limit access to the computer.
Exit	For saving or discarding changes.
Setup Subscreen	Description
Floppy Options	For configuring your diskette drives.
IDE Device Configuration	For configuring your IDE devices.
Boot Options	For modifying options that affect the computer boot up, such as the boot sequence.
Peripheral Configuration	For modifying options that affect the serial ports, the parallel port, and the disk drive interfaces.
Advanced Chipset Configuration	For modifying options that affect memory and peripheral busses.
Power Management Configuration	For accessing and modifying Advanced Power Management (APM) options.
Plug and Play Configuration	For modifying options that affect the system's Plug and Play capabilities.

3.12.2 Main Setup Screen

This section describes the Setup options found on the main menu screen. If you select certain options from the main screen (e.g., Hard Disk), the Setup program switches to a subscreen for the selected option.

3.12.2.1 System Date

Specifies the current date. Select the month from a pop-up menu.

3.12.2.2 System Time

Specifies the current time.

3.12.2.3 Floppy Options

When selected, this pops up the Floppy Options menu.

3.12.2.4 Primary Master

Reports if an IDE device is connected to the motherboard. When selected, this brings up the IDE Device Configuration subscreen.

3.12.2.5 Primary Slave

Reports if an IDE device is connected to the motherboard. When selected, this brings up the IDE Device Configuration subscreen.

3.12.2.6 Secondary Master

Reports if an IDE device is connected to the motherboard. When selected, this brings up the IDE Device Configuration subscreen.

3.12.2.7 Secondary Slave

Reports if an IDE device is connected to the motherboard. When selected, this brings up the IDE Device Configuration subscreen.

3.12.2.8 Language

Specifies the language of the text strings used in the Setup program and the BIOS. The options are any installed languages.

3.12.2.9 Boot Options

When selected, this brings up the Boot Options subscreen.

3.12.2.10 Video Mode

Reports the video mode. There are no options.

3.12.2.11 Mouse

Reports if a mouse is installed or not. There are no options.

3.12.2.12 Base Memory

Reports the amount of base memory. There are no options.

3.12.2.13 Extended Memory

Reports the amount of extended memory. There are no options.

3.12.3 Floppy Options Subscreen

3.12.3.1 Floppy A:

Reports if a diskette drive is connected to the motherboard. There are no options.

3.12.3.2 Floppy B:

Reports if a second diskette drive is connected to the motherboard. There are no options.

3.12.3.3 Floppy A: Type

Specifies the physical size and capacity of the diskette drive. The options are Disabled, 360 KB, 5.25-inch; 1.2 MB, 5.25-inch; 720 KB, 3.5-inch; 1.44/1.25 MB, 3.5-inch; 2.88 MB, 3.5-inch. The default is 1.44/1.25 MB, 3.5-inch.

3.12.3.4 Floppy B: Type

Specifies the physical size and capacity of the diskette drive. The options are Disabled, 360 KB, 5.25-inch; 1.2 MB, 5.25-inch; 720 KB, 3.5-inch; 1.44/1.25 MB, 3.5-inch; 2.88 MB, 3.5-inch. The default is Disabled.

3.12.3.5 Floppy Access

Specifies read/write access for all attached floppy drives. The options are Read/Write and Read Only. The default is Read/Write.

3.12.4 IDE Device Configuration Subscreen

3.12.4.1 IDE Device Configuration

Used to manually configure the hard drive or have the BIOS auto configure it. The options are Auto Configured, User Definable and Disabled. The default is Auto Configured. If you select User Definable then the Number of Cylinders, Number of Heads, and Number of Sectors items can be modified.

3.12.4.2 Number of Cylinders

If IDE Device Configuration is set to User Definable, you must type the correct number of cylinders for your hard disk. If Hard Disk Type is set to Auto Configured, this reports the number of cylinders for your hard disk and cannot be modified.

3.12.4.3 Number of Heads

If IDE Device Configuration is set to User Definable, you must type the correct number of heads for your hard disk. If Hard Disk Type is set to Auto Configured, this reports the number of heads for your hard disk and cannot be modified.

3.12.4.4 Number of Sectors

If IDE Device Configuration is set to User Definable, you must type the correct number of sectors for your hard disk. If Hard Disk Type is set to Auto Configured, this reports the number of sectors for your hard disk and cannot be modified.

3.12.4.5 Maximum Capacity

Reports the maximum capacity of your IDE Device. It is calculated from the number of cylinders, heads, and sectors. There are no options here.

3.12.4.6 IDE Translation Mode

Specifies the IDE translation mode. The options are Standard CHS (standard cylinder head sector—less than 1024 cylinders), Logical Block, Extended CHS (extended cylinder head sector—greater than 1024 cylinders), and Auto Detected (BIOS detects IDE drive support for LBA). The default is Auto Detected.



CAUTION

Do not change this from the option selected when the hard drive was formatted. Changing the option can result in corrupted data.

3.12.4.7 Multiple Sector Setting

Sets the number of sectors transferred by an IDE drive per interrupt generated. The options are Disabled, 4 Sectors/Block, 8 Sectors/Block, or Auto Detected. The default is Auto Detected. Check the specifications for your hard disk drive to determine which setting provides optimum performance for your drive.

3.12.4.8 Fast Programmed I/O Modes

Sets how fast transfers on the IDE interface occur. The options are Disabled or Auto Detected. The default is Auto Detected. If set to Disabled, transfers occur at a less than optimized speed. If set to Auto Detected, transfers occur at the drive's maximum speed.

3.12.5 Boot Options Subscreen

This section describes the options available on the Boot Options subscreen.

3.12.5.1 First, Second, Third, Fourth Boot Device

Sets which drives the BIOS checks to find an operating system to boot from. The following options are available:

First Boot Device:	Select Disabled, Floppy, Hard Disk, CD-ROM, Network.
Second, Third, Fourth Device:	Select Disabled, Floppy, Hard Disk, Network.

3.12.5.2 System Cache

Enables or disables both the primary and the secondary cache memory. The options are Enabled or Disabled. The default is Enabled.

3.12.5.3 Boot Speed

Sets the system's boot speed. The options are Deturbo and Turbo. The default is Turbo. If Turbo is selected, boot-up occurs at full speed. If Deturbo is selected, the board operates at a slower speed.

3.12.5.4 Num Lock

Sets the beginning state of the Num Lock feature on your keyboard. The options are On and Off. The default is Off.

3.12.5.5 Setup Prompt

Turns on (or off) the “Press <F1> Key if you want to run Setup” prompt during the power-up sequence. The options are Enabled and Disabled. The default is Enabled.

⇒ **NOTE**

This option has no effect on your ability to access the Setup program. It only toggles the prompt.

3.12.5.6 Typematic Rate Programming

Sets the typematic rates. The options are Default and Override. The default is Default. Choosing Override enables Typematic Rate Delay and Typematic Rate.

3.12.5.7 Typematic Rate Delay

Sets how long it takes for the key-repeat function to start when you hold down a key on the keyboard. The options are 250, 500, 750, and 1000 millisecond delays. The default is 250. If Typematic Rate Programming is set to Default, this option will not be visible.

3.12.5.8 Typematic Rate

Sets the speed at which characters repeat when you hold down a key on the keyboard. The higher the number, the faster the characters repeat. The options are 6, 8, 10, 12, 15, 20, 24, and 30 characters per second. The default is 6. If Typematic Rate Programming is set to Default, this option will not be visible.

3.12.6 Advanced Screen

This section describes the Setup options found on the Advanced menu screen. If you select certain options from the Advanced screen (e.g., Peripheral Configuration), the Setup program switches to a subscreen for the selected option. Subscreens are described in the sections following the description of the Advanced screen options.

3.12.6.1 Processor Type

Reports the microprocessor type. There are no options.

3.12.6.2 Processor Speed

Reports the microprocessor clock speed. There are no options.

3.12.6.3 Cache Size

Reports the size of the secondary cache. There are no options. If your motherboard contains no L2 cache, this item will not appear.

3.12.6.4 Peripheral Configuration

When selected, this brings up the Peripheral Configuration subscreen.

3.12.6.5 Advanced Chipset Configuration

When selected, this brings up the Advanced Chipset Configuration subscreen.

3.12.6.6 Power Management Configuration

When selected and enabled, this brings up the Advanced Power Management subscreen.

3.12.6.7 Plug and Play Configuration

When selected, this brings up the Plug and Play Configuration subscreen.

3.12.7 Peripheral Configuration Subscreen

This section describes the screens for the peripheral configuration subscreen.

3.12.7.1 Configuration Mode

Enables you to choose between setting the peripheral configuration yourself, or having the BIOS do it. The options are Auto and Manual. The default is Auto.

When Auto is selected, the peripherals are automatically configured during power up. The options below for PCI IDE Interface, Floppy Interface, Serial Port 1 and Serial Port 2 Addresses, Serial Port 2 IR Mode, and the Parallel Port Address cannot be modified. The settings displayed for those options reflect the current state of the hardware.

3.12.7.2 PCI IDE Interface

Enables or disables the PCI IDE hard disk interface. The options are Enabled and Disabled. The default is Enabled. (If Configuration Mode is set to Auto, this option cannot be modified.)

3.12.7.3 Floppy Interface

Enables or disables the diskette drive interface. The options are Enabled and Disabled. The default is Enabled. (If Configuration Mode is set to Auto, this option cannot be modified.)

3.12.7.4 Serial Port 1 Address

Selects the address of the serial port. The options are Disabled; COM1, 3F8h; COM2, 2F8h; COM3, 3E8h; and COM4, 2E8h. The default is COM1, 3F8h. If the Configuration Mode is set to Auto, the Setup program assigns the first free COM port (normally COM1, 3F8h) as the serial port 1 address, regardless of what is selected under the Serial Port 1 Address option. (If Configuration Mode is set to Auto, this option cannot be modified.)

3.12.7.5 Serial Port 2 Address

Selects the address of the serial port. The options are Disabled; COM1, 3F8h; COM2, 2F8h; COM3, 3E8h; and COM4, 2E8h. The default is COM2, 2F8h. If the Configuration Mode is set to Auto, the Setup program assigns the first free COM port (normally COM2, 2F8h) as the serial port 2 address, regardless of what is selected under the Serial Port 2 Address option. (If Configuration Mode is set to Auto, this option cannot be modified.)

⇒ **NOTE**

If either serial port address is set, the address it is set to will not appear in the options dialog box of the other serial port. If an ATI mach32[†] or an ATI mach64[†] video controller is active, the COM4, 2E8h address will not appear in the options dialog box of either serial port.

3.12.7.6 Serial Port 2 IR Mode

Makes Serial Port 2 available to infrared applications. The options are Enabled and Disabled. The default is Disabled. (If Configuration Mode is set to Auto, this option cannot be modified.)

3.12.7.7 Parallel Port Address

Selects the address and IRQ of the parallel port. The options are Disabled; LPT3, 3BCh, IRQ7; LPT1, 378h, IRQ7; LPT1, 378h, IRQ5; and LPT2, 278h, IRQ5. The default is LPT1, 378h, IRQ7. If the Configuration Mode is set to Auto, the Setup program assigns LPT1, 378h, IRQ7 as the parallel port address, regardless of what is selected under the Parallel Port Address option. (If Configuration Mode is set to Auto, this option cannot be modified.)

3.12.7.8 Parallel Port Mode

Selects the mode for the parallel port. The options are Compatible, Bidirectional, EPP, and ECP. The default is Compatible. Compatible means the parallel port operates in AT-compatible mode. Bidirectional means the parallel port operates in bidirectional PS/2-compatible mode. EPP and ECP mean the parallel port operates high-speed, bidirectionally. This option is not affected by the Configuration Mode field above.

3.12.8 Advanced Chipset Configuration Subscreen

This section describes the options available on the Advanced Chipset Configuration Subscreen.

3.12.8.1 Base Memory Size

Sets the size of the base memory. The options are 512 KB and 640 KB. The default is 640 KB.

3.12.8.2 ISA LFB Size

Sets the size of the linear frame buffer. The options are Disabled and 1 MB. The default is Disabled. If this is set to 1 MB, then the ISA LFB Base Address field will appear.

3.12.8.3 ISA LFB Base Address

Reports the base address of the LFB. There are no options. This field will not appear if the ISA LFB Size is set to Disabled.

3.12.8.4 Video Palette Snoop

Controls the ability of a primary PCI graphics controller to share a common palette with an ISA add-in video card. The options are Enabled and Disabled. The default is Disabled.

3.12.8.5 Latency Timer (PCI Clocks)

Sets the length of time an agent on the PCI bus can hold the bus when another agent has requested the bus. Valid numbers are between 0 and 256. The default is 66.

3.12.8.6 PCI Burst

Controls the support for PCI to memory burst mode data transfers. The options are Enabled and Disabled. The default is Enabled.

3.12.9 Power Management Configuration Subscreen

This section describes the options available on the Power Management Subscreen.

3.12.9.1 Advanced Power Management

Enables or disables the Advanced Power Management (APM) support in your system's BIOS. The options are Enabled and Disabled. The default is Enabled. Power Management will only work with APM-capable operating systems. If Advanced Power Management is set to Disabled, none of the fields in the Advanced Power Management subscreen will be visible.

3.12.9.2 IDE Drive Power Down

Sets any IDE drives to spin down when the computer goes into power managed mode. The options are Enabled and Disabled. The default is Enabled.

3.12.9.3 Inactivity Timer

Sets how long the computer must be inactive before it enters power managed mode. Enter the number of minutes. The range is 0 to 255 minutes. The default is 10 minutes.

3.12.9.4 VESA Video Power Down

Sets the command issued to your graphics card when the computer goes into power managed mode. The options are Disabled, Standby, Suspend, and Sleep. The default is Sleep.

3.12.9.5 Hot Key

Sets the hot key that, when pressed while holding down the <Ctrl> and <Alt> keys, causes the computer to enter power managed mode. All alphabetic keys are valid.

3.12.10 Plug and Play Configuration Subscreen

This section describes the options found on the Plug and Play configuration subscreen.

3.12.10.1 Configuration Mode

Sets how the BIOS gets information about ISA cards that do not have Plug and Play capabilities. The options are Use Setup program and Use ICU (ISA Configuration Utility). The default is Use Setup program.

If Use ICU is selected, the BIOS will depend on run-time software to ensure that there are no conflicts between ISA boards with Plug and Play capabilities and those without. Only Boot With PnP OS will be visible.

3.12.10.2 Boot with PnP OS

Enables the PC to boot with an operating system capable of managing Plug and Play add-in cards. The options are None, Other, and Windows 95. The default is Windows 95.

3.12.10.3 ISA Shared Memory Size

Enables you to specify a range of memory addresses that will be directed to the ISA bus rather than on-board memory. The options are Disabled, 16 KB, 32 KB, 48 KB, 64 KB, 80 KB, and 96 KB. The default is Disabled. If this is set to Disabled, the ISA Shared Memory Base Address (described below) will not be visible. This field should be set to Enabled only when a non Plug and Play ISA card (legacy card) that requires non-ROM memory space is used. LAN cards that have on-board memory buffers are one example of this; video capture cards that have video buffer memory are another. By default, allocation of upper memory is as follows: memory from C0000-C7FFF is automatically shadowed. (This memory range is typically reserved for video BIOS.) Memory from C8000-DFFFFh is initially unshadowed. The BIOS scans this range for any ISA expansion card BIOSes that may be present and notes their location and size. The BIOS will then autoconfigure the PCI and Plug and Play devices, shadowing the ROM requirements (other than video) into the area above E0000h until that area is full. It will then assign additional PCI and Plug and Play expansion cards to the area between C8000h and DFFFFh. If an ISA legacy card has non-ROM memory requirements, the autoconfigure routine may write into an area that is needed by the ISA expansion card. The ISA Shared Memory Size parameter signifies the autoconfigure routine that this block of memory is reserved and should not be shadowed.

Shadowing is a technique that copies a block of memory from an add-in card's ROM to the same address in main memory. This provides faster access and achieves higher performance. By default, all upper memory is shadowed.

3.12.10.4 ISA Shared Memory Base Address

Sets the base address for the ISA Shared Memory. The options are C8000h, CC000h, D0000h, D4000h, D8000h, and DC000h. The default is C8000h. This setting could affect the ISA Shared Memory Size item. The value entered in the ISA Shared Memory Size item cannot extend to the E0000h address. For example, if a size of 64KB was selected, options D4000h, D8000h, and DC000h will not be available.

3.12.10.5 IRQ 3, 4, 5, 7, 9, 10, 11, 12, 14, 15

Sets the status of the IRQ. The options are Available and Used By ISA Card. The default is Available. The PCI auto-configuration code looks here to see if these interrupts are available for use by a PCI or Plug and Play device. If an interrupt is available, the PCI auto-configuration code or the Plug and Play agent can assign the interrupt to the device. If your computer contains an ISA agent that uses one of these interrupts, select Used By ISA Card for that interrupt.

⇒ **NOTE**

IRQ 3, 4, 5, and 7 may not be available in this option, depending on the setting chosen for the COM1, COM2 and parallel ports in the Peripheral Configuration Subscreen.

IRQ 14 and 15 will not show up as user available. If the on-board IDE controller is disabled, these interrupts will be available to ISA cards. These interrupts can not be used for PCI cards

3.12.11 Security Screen

This section describes the two access modes that can be set using the options found on the Security screen, and then describes the Security screen options themselves.

3.12.11.1 Administrative and User Access Modes

The options on the Security screen menu make it possible to restrict access to the Setup program by enabling you to set passwords for two different access modes: Administrative mode and User mode.

In general, Administrative mode has full access to the Setup options, whereas User mode has restricted access to the options. Thus, by setting separate Administrative and User passwords, a system administrator can limit who can change critical Setup values. The actual limitations depend on whether either the Administrative or User passwords or both are set. (See the table below for a description of how the passwords actually work together.)

To limit access to who can boot the computer, set the User password. This is the password that the computer asks for before booting. If only the Administrative password is set, the computer boots up without asking for a password. If both passwords are set, you can enter either password to boot the computer.

The following table shows the effects of setting the Administrative and User passwords. (The table is for reference only, and is not shown on the Security screen.) In the table, the statement “Can change a limited number of options” means you can change the system date and time, the power management hot key, the User password, the security hot key, and unattended start.

Table 13. Administrative and User Password Functions

Password Set	Administrative mode can . . .	User mode can . . .	Password Required During Boot Process
Neither	Can change all options*	Can change all options*	None
Administrative only	Can change all options	Can change a limited number of options	None
User only	N/A	Can change all options	User
Both	Can change all options	Can change a limited number of options	Administrative or User

* If no password is set, any user can change all Setup options.

3.12.12 Security Screen Options

3.12.12.1 User Password is

Reports if there is a User password set. There are no options.

3.12.12.2 Administrative Password is

Reports if there is an Administrative password set. There are no options.

3.12.12.3 Set User Password

Sets the User password. The password can be up to seven alphanumeric characters.

3.12.12.4 Set Administrative Password

Sets the Administrative password. The password can be up to seven alphanumeric characters.

3.12.12.5 Unattended Start

Controls when the security password is requested. The options are Enabled and Disabled. The default is Disabled. The User password must be enabled before you can enable this option. If Enabled is selected, the computer boots, but the keyboard will be locked until the User password is entered.

3.12.12.6 Security Hot Key (CTRL-ALT-)

Sets a hot key that, when pressed, locks the keyboard until the User password is entered. The Keyboard LEDs flash to indicate that the keyboard is locked. When you enter the User password, you do not have to press the <Enter> key.

3.12.13 Exit Screen

This section describes the different ways to exit and save or not save changes made in the Setup program.

3.12.13.1 Exit Saving Changes

Saves the changes to CMOS RAM and exits the Setup program. You can also press the <F10> key anywhere in the Setup program to do this.

3.12.13.2 Exit Discarding Changes

Exits the Setup program without saving any changes. This means that any changes made while in the Setup program are discarded and NOT SAVED. Pressing the <Esc> key in any of the four main screens will do this.

3.12.13.3 Load Setup Defaults

Resets all of the Setup options to their defaults. You can also press the <F5> key anywhere in the Setup program to do this.

This selection loads the default Setup values from the ROM table.

3.12.13.4 Discard Changes

Discards any changes you made during the current Setup session without exiting the program. You can also press the <F6> key anywhere in the Setup program to do this.

This selection loads the CMOS RAM values that were present when the computer was turned on.

4 Error Messages and Beep Codes

4.1 BIOS Beep Codes

Beeps	Error Message	Description
1	Refresh Failure	The memory refresh circuitry on the motherboard is faulty.
3	Base 64 KB Memory Failure	Memory failure in the first 64 KB.
4	Timer Not Operational	Memory failure in the first 64 KB of memory, or Timer 1 on the motherboard is not functioning.
5	Processor Error	The microprocessor on the motherboard generated an error.
6	Gate A20 Failure	The keyboard controller may be bad. The BIOS cannot switch to protected mode.
7	Processor Exception Interrupt Error	The microprocessor generated an exception interrupt.
8	Display Memory Read/Write Error	The video adapter is either missing or its memory is faulty. This is not a fatal error.
9	ROM Checksum Error	ROM checksum value does not match the value encoded in BIOS.
10	CMOS Shutdown Register Rd/Wrt Error	The shutdown register for CMOS RAM failed.

4.2 PCI Configuration Error Messages

The following PCI messages are displayed as a group with bus, device and function information.

Message	Explanation
Bad PnP Serial ID Checksum	The Serial ID checksum of a Plug and Play card was invalid.
Floppy Disk Controller Resource Conflict	The floppy disk controller has requested a resource that is already in use.
NVRAM Checksum Error, NVRAM Cleared	The ESCD data was reinitialized because of an NVRAM checksum error. Try rerunning the ICU.
NVRAM Cleared By Jumper	The "Clear CMOS" jumper has been moved to the "Clear" position and CMOS RAM has been cleared.
NVRAM Data Invalid, NVRAM Cleared	Invalid entry in the ESCD.
Parallel Port Resource Conflict	The parallel port has requested a resource that is already in use.
PCI Error Log is Full	This message is displayed when more than 15 PCI conflict errors are detected. No additional PCI errors can be logged.
PCI I/O Port Conflict	Two devices requested the same resource, resulting in a conflict.

continued 

PCI Configuration Error Messages (continued)

Message	Explanation
PCI IRQ Conflict	Two devices requested the same resource, resulting in a conflict.
PCI Memory Conflict	Two devices requested the same resource, resulting in a conflict.
Primary Boot Device Not Found	The designated primary boot device (Floppy, hard disk drive, CD-ROM drive, or Network) could not be found.
Primary IDE Controller Resource Conflict	The primary IDE controller has requested a resource that is already in use.
Primary Input Device Not Found	The designated primary input device (keyboard, mouse, or other, if input is redirected) could not be found.
Secondary IDE Controller Resource Conflict	The secondary IDE controller has requested a resource that is already in use.
Serial Port 1 Resource Conflict	Serial port 1 has requested a resource that is already in use.
Serial Port 2 Resource Conflict	Serial port 2 has requested a resource that is already in use.
Static Device Resource Conflict	A non Plug and Play ISA card has requested a resource that is already in use.
System Board Device Resource Conflict	A non Plug and Play ISA card has requested a resource that is already in use.

4.3 BIOS Error Messages

Error Message	Explanation
Gate A20 Error	Gate A20 on the keyboard controller is not working.
Address Line Short!	Error in the address decoding circuitry on the motherboard.
Cache Memory Bad, Do Not Enable Cache!	Cache memory is defective. Replace it.
CH-2 Timer Error	Most systems include two timers. There is an error in timer 2.
CMOS Battery State Low	The battery power is low. Replace the battery.
CMOS Checksum Failure	After CMOS RAM values are saved, a checksum value is generated for error checking. The previous value is different from the current value. Run Setup.
CMOS System Options Not Set	The values stored in CMOS RAM are either corrupt or nonexistent. Run Setup.
CMOS Display Type Mismatch	The video type in CMOS RAM does not match the type detected by the BIOS. Run Setup.
CMOS Memory Size Mismatch	The amount of memory on the motherboard is different than the amount in CMOS RAM. Run Setup.
CMOS Time and Date Not Set	Run Setup to set the date and time in CMOS RAM.

continued 

BIOS Error Messages (continued)

Error Message	Explanation
Diskette Boot Failure	The boot disk in floppy drive A: is corrupt. It cannot be used to boot the computer. Use another boot disk and follow the screen instructions.
Display Switch Not Proper	The display jumper is not implemented on this product, this error will not occur.
DMA Error	Error in the DMA controller.
DMA#1 Error	Error in the first DMA channel.
DMA#2 Error	Error in the second DMA channel.
FDD Controller Failure	The BIOS cannot communicate with the floppy disk drive controller. Check all appropriate connections after the computer is powered down.
HDD Controller Failure	The BIOS cannot communicate with the hard disk drive controller. Check all appropriate connections after the computer is powered down.
INTR#1 Error	Interrupt channel 1 failed POST.
INTR#2 Error	Interrupt channel 2 failed POST.
Invalid Boot Diskette	The BIOS can read the disk in floppy drive A:, but cannot boot the computer. Use another boot disk.
Keyboard Is Locked...Unlock It	The keyboard lock on the computer is engaged. The computer must be unlocked to continue.
KB/Interface Error	There is an error in the keyboard connector.
Off Board Parity Error	Parity error in memory installed in an expansion slot. The format is: OFF BOARD PARITY ERROR ADDR (HEX) = (XXXX) XXXX is the hex address where the error occurred.

4.4 ISA NMI Messages

ISA NMI Message	Explanation
I/O Card Parity Error at xxxxx	An expansion card failed. If the address can be determined, it is displayed as xxxxx. If not, the message is I/O Card Parity Error ????.
DMA Bus Time-out	A device has driven the bus signal for more than 7.8 microseconds.

