intel®

TC430HX
Motherboard
Specification Update

Release Date: January 1998

Order Number: 281826-015

The TC430HX motherboard may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are documented in this Specification Update.

CONTENTS

Specification Update for TC430HX Motherboards

REVISION HISTORY

Date of Revision	Version	Description
August 1996	-001	This document is the first Specification Update for the Intel TC430HX motherboard.
September 1996	-002	Added Erratum 3 and Documentation Changes 1-2.
October 1996	-003	Added Documentation Changes 3-6.
November 1996	-004	Added Erratum 4, Documentation Changes 7-11 and Updated Errata 2-3.
December 1996	-005	Added Errata 5-8, Specification Clarification 1 and Documentation Changes 12-13.
January 1997	-006	Added Erratum 9, Specification Clarification 2, Documentation Changes 14-16 and PBA/BIOS Table.
February 1997	-007	Added Documentation Changes 17-20.
March 1997	-008	Added AA Revision to Motherboard Identification table. Revised format of PBA/BIOS revision table. Updated Errata 1-2. Added Erratum 10. Removed Specification Clarifications 1-2 and Documentation Changes 1-20, which were incorporated into revision -002 of the specification.
April 1997	-009	Updated Erratum 7. Added Erratum 11 and Documentation Change 1.
May 1997	-010	Updated Erratum 9 and Added Erratum 12.
June 1997	-011	Added Specification Change 1, Errata 13-14, Specification Clarifications 1-2 and Documentation Changes 2-3. Updated Errata 4 and 10.
July 1997	-012	Added Specification Changes 2-3 and Documentation Changes 4-9.
August 1997	-013	Added Specification Clarification 3 and Documentation Changes 10-11.
October 1997	-014	Added Documentation Changes 12-14.
January 1998	-015	Updated Specification Change 3 and Documentation Change 1. Added Errata 15-16.

PREFACE

This document is an update to the specifications contained in the *TC430HX Motherboard Technical Product Specification* (Order Number 281820). It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools. It will contain Specification Changes, Errata, Specification Clarifications, and Documentation Changes.

Refer to the *Pentium® Processor Specification Update* (Order Number 242480) for specification updates concerning the Pentium processor. Items contained in the *Pentium Processor Specification Update* that either do not apply to the TC430HX motherboard or have been worked around are noted in this document. Otherwise, it should be assumed that any processor errata for a given stepping are applicable to the Printed Board Assembly (PBA) revision(s) associated with that stepping.

Refer to the *82430HX PCIset Specification Update* (Order Number 297652) for specification updates concerning the 82430HX PCIset. Items contained in the *82430HX PCIset Specification Update* that either do not apply to the TC430HX motherboard or have been worked around are noted in this document. Otherwise, it should be assumed that any PCIset errata for a given stepping are applicable to the Printed Board Assembly (PBA) revision(s) associated with that stepping.

Refer to the *82371SB PIIX3 Specification Update* (Order Number 297658) for specification updates concerning the 82371SB PIIX3. Items contained in the *82371SB PIIX3 Specification Update* that either do not apply to the TC430HX motherboard or have been worked around are noted in this document. Otherwise, it should be assumed that any PCIset errata for a given stepping are applicable to the Printed Board Assembly (PBA) revision(s) associated with that stepping.

Nomenclature

Specification Changes are modifications to the current published specifications. These changes will be incorporated in the next release of the specifications.

Errata are design defects or errors. Characterized errata may cause the TC430HX motherboard's behavior to deviate from published specifications. Hardware and software designed to be used with any given Printed Board Assembly (PBA) and BIOS revision level must assume that all errata documented for that PBA and BIOS revision are present on all motherboards.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.

Documentation Changes include typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.

**Specification Update for
TC430HX Motherboards**

GENERAL INFORMATION

Basic TC430HX Motherboard Identification Information

AA Revision	PBA Revision	82430HX PCIset Stepping	BIOS Revision	Notes
659120-302	659122-302	A1	1.00.01.DH0	1, 2, 3, 4, 8
659120-303	659122-303	A1	1.00.01.DH0	1, 2, 3, 4, 8
659120-304 661449-304	659122-304	A1	1.00.02.DH0	1, 2, 3, 4, 8
659120-502 661449-502	659122-502	A1	1.00.02.DH0	1, 2, 3, 4, 8
659120-503 661449-503	659122-503	A3	1.00.04.DH0	1, 5, 6, 7, 8
659120-504 661449-504	659122-504	A3	1.00.04.DH0	1, 5, 6, 7, 8
659120-505 661449-505	659122-505	A3	1.00.05.DH0	1, 5, 6, 7, 8
659120-602 661449-602	659122-602	A3	1.00.05.DH0	1, 5, 6, 7, 8
659120-603 661449-603	659122-603	A3	1.00.05.DH0	1, 5, 6, 7, 8
664190-502	663350-502	A3	1.00.04.DH0	1, 5, 6, 7, 8
664190-503	663350-503	A3	1.00.04.DH0	1, 5, 6, 7, 8
664190-504	663350-504	A3	1.00.05.DH0	1, 5, 6, 7, 8
664190-602	663350-602	A3	1.00.05.DH0	1, 5, 6, 7, 8
664190-603	663350-603	A3	1.00.05.DH0	1, 5, 6, 7, 8
666740-601	666736-601	A3	1.00.05.DH0	1, 5, 6, 7, 8
666740-602	666736-602	A3	1.00.05.DH0	1, 5, 6, 7, 8
666741-601	666737-601	A3	1.00.05.DH0	1, 5, 6, 7, 8
666741-602	666737-602	A3	1.00.05.DH0	1, 5, 6, 7, 8
666741-603	666737-603	A3	1.00.06.DH0	1, 5, 6, 7, 8
668222-601	668221-601	A3	1.00.05.DH0	1, 5, 6, 7, 8
668222-602	668221-602	A3	1.00.05.DH0	1, 5, 6, 7, 8
677269-602	677266-602	A3	1.00.05.DH0	1, 5, 6, 7, 8
677269-603	677266-603	A3	1.00.07.DH0	1, 5, 6, 7, 8
677269-604	677266-604	A3	1.00.07.DH0	1, 5, 6, 7, 8
677270-603	677267-603	A3	1.00.06.DH0	1, 5, 6, 7, 8
677270-604	677267-604	A3	1.00.07.DH0	1, 5, 6, 7, 8

AA Revision	PBA Revision	82430HX PCIset Stepping	BIOS Revision	Notes
677270-605	677267-605	A3	1.00.07.DH0	1, 5, 6, 7, 8

NOTES:

1. The AA/PBA number is found on a small label on the component side of the board.

2. The 82430HX PCIset kit used on this PBA revision consists of two different components as follows:

Device	Stepping	S-Spec Numbers
82439HX	A1	SU087
82371SB	B0	SU093

3. The following errata contained in the *82430HX PCIset Specification Update* (Order Number 297652) either do not apply to the TC430HX motherboard or have been worked around in this PBA and/or BIOS revision. All other errata associated with the PCIset apply to this PBA revision. For specific details of any erratum please refer to the *82430HX PCIset Specification Update*.

4. The following errata contained in the *82371SB PIIX3 Specification Update* (Order Number 297658) either do not apply to the TC430HX motherboard or have been worked around in this PBA and/or BIOS revision: 2-12. All other errata associated with the PCIset apply to this PBA revision. For specific details of any erratum please refer to the *82371SB PIIX3 Specification Update*.

5. The 82430HX PCIset kit used on this PBA revision consists of two different components as follows:

Device	Stepping	S-Spec Numbers
82439HX	A3	SU115
82371SB	B0	SU093

6. The following errata contained in the *82430HX PCIset Specification Update* (Order Number 297652) either do not apply to the TC430HX motherboard or have been worked around in this PBA and/or BIOS revision. All other errata associated with the PCIset apply to this PBA revision. For specific details of any erratum please refer to the *82430HX PCIset Specification Update*.

7. The following errata contained in the *82371SB PIIX3 Specification Update* (Order Number 297658) either do not apply to the TC430HX motherboard or have been worked around in this PBA and/or BIOS revision: 1-7. All other errata associated with the PCIset apply to this PBA revision. For specific details of any erratum please refer to the *82371SB PIIX3 Specification Update*.

8. The following errata contained in Part I of the *Pentium® Processor Specification Update* (Order Number 242480) either do not apply to the TC430HX motherboard or have been worked around in this PBA and/or BIOS revision: 5, 7, 9-11, 13-14, 16-17, 29, 31, 34, 36-37, 39, 40, 46, 48-50, 58, 60-64, 66-67, 69, 71, all DP errata, all AP errata, all TCP errata. All other errata in Part I may apply to this revision level of the motherboard, depending on the stepping of the processor or the specific software that is being executed. Also, some of these errata apply only to motherboards being used in an application development environment. For specific details of any erratum please refer to the *Pentium Processor Specification Update*.

Summary Table of Changes

The following table indicates the Specification Changes, Errata, Specification Clarifications, or Documentation Changes which apply to the TC430HX motherboard. Intel intends to fix some of the errata in a future revision of the motherboard, and to account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

CODES USED IN SUMMARY TABLE

Doc:	Document change or update that will be implemented.
Fix:	This erratum is intended to be fixed in a future revision of the motherboard or BIOS.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.
Shaded:	This erratum is either new or modified from the previous version of the document.

NO.	PLANS	SPECIFICATION CHANGES
1	Doc	Support for 233 MHz Pentium® processors with MMX™ technology
2	Doc	User password clear feature
3	Doc	LS-120 drive support

NO.	PLANS	ERRATA
1	Fixed	ECC non-detection of single/double bit errors on partial memory writes
2	Fixed	PCI Delayed Transactions are not supported
3	Fix	MIDI to WAV recording may result in distortion on playback
4	Fixed	BIOS does not support no-emulation mode for CD-ROM boot
5	Fix	System BIOS does not recognize bootable USB devices
6	NoFix	USB voltage may drop below 4.75 volts
7	Fixed	CMOS checksum may be lost if power is cycled during boot
8	NoFix	PCI device scan may terminate abnormally
9	NoFix	PCI add-card may hang system due to improper TRST# signal
10	NoFix	Slave on secondary IDE channel is not disabled
11	NoFix	Cannot meet FCC Class B requirements using unshielded USB cable
12	NoFix	Audio driver does not support Windows* 3.x session within OS/2* Warp*
13	Fixed	System BIOS does not allocate IRQ resources to PCI video cards
14	Fixed	System BIOS may assign conflicting resources for parallel port
15	NoFix	System BIOS may corrupt audio add-in card EEPROM
16	Fixed	MIDI playback not available in OS/2 Warp 3.0

NO.	PLANS	SPECIFICATION CLARIFICATIONS
1	Doc	Advanced Power Management (APM) will not function as expected with Universal Serial Bus (USB) enabled
2	Doc	PCI 2.1 Specification optional features
3	Doc	Power supply considerations
NO.	PLANS	DOCUMENTATION CHANGES
1	Doc	Revision of Section 1.10.12.1, "Speaker"
2	Doc	Revision of Section 1.2, "Motherboard Manufacturing Options"
3	Doc	Revision of Section 1.10.13.2, "Wavetable Upgrade"
4	Doc	Revision of Section 1.6.1, "Xcelerated Controller (TXC)"
5	Doc	Revision of Section 1.10.10, "PCI Connectors – J4C1, J4D1, J4D2, J4E1"
6	Doc	Addition of Onboard Video IRQ Section
7	Doc	Revision of Section 3.12.12, "Security Screen"
8	Doc	Revision of Section 3.12.3.3, "Floppy A: Type"
9	Doc	Revision of Section 3.12.3.4, "Floppy B: Type"
10	Doc	Revision of Section 1.11.3, "Clear CMOS (J10C1-A, Pins 4, 5 and 6)"
11	Doc	Addition of " Power Supply Considerations" section
12	Doc	Revision of Section 1.9, "Audio Subsystem"
13	Doc	Revision of Section 1.10.14.3, "Serial Port Connector"
14	Doc	Revision of Section 1.11.1, "Microprocessor Configuration (J10C1-C, D)"

The errata described in this specification update apply to combinations of PBA revision and BIOS revision as shown in the table below. Descriptions of the individual errata referred to by number in the table below are found in the ERRATA section of this document.

PBA Revision	BIOS Revision	Errata That Apply
659122-302	1.00.01.DH0	1-16
	1.00.02.DH0	1-16
	1.00.04.DH0	1-16
	1.00.05.DH0	1-6, 8-16
	1.00.06.DH0	1-6, 8-16
	1.00.07.DH0	1-3, 5, 8-12, 16

PBA Revision	BIOS Revision	Errata That Apply
659122-303	1.00.01.DH0	1-16
	1.00.02.DH0	1-16
	1.00.04.DH0	1-16
	1.00.05.DH0	1-6, 8-16
	1.00.06.DH0	1-6, 8-16
	1.00.07.DH0	1-3, 5, 8-12, 16
659122-304	1.00.01.DH0[‡]	1-16
	1.00.02.DH0	1-16
	1.00.04.DH0	1-16
	1.00.05.DH0	1-6, 8-16
	1.00.06.DH0	1-6, 8-16
	1.00.07.DH0	1-3, 5, 8-12, 16
659122-502	1.00.01.DH0[‡]	1-16
	1.00.02.DH0	1-16
	1.00.04.DH0	1-16
	1.00.05.DH0	1-6, 8-16
	1.00.06.DH0	1-6, 8-16
	1.00.07.DH0	1-3, 5, 8-12, 16
659122-503	1.00.01.DH0[‡]	1-16
	1.00.02.DH0[‡]	1-16
	1.00.04.DH0	3-16
	1.00.05.DH0	3-6, 8-16
	1.00.06.DH0	3-6, 8-16
	1.00.07.DH0	3, 5-6, 8-12, 16
659122-504	1.00.01.DH0[‡]	1-16
	1.00.02.DH0[‡]	1-16
	1.00.04.DH0	3-16
	1.00.05.DH0	3-6, 8-16
	1.00.06.DH0	3-6, 8-16
	1.00.07.DH0	3, 5-6, 8-12, 16

PBA Revision	BIOS Revision	Errata That Apply
659122-505	1.00.01.DH0‡	1-16
	1.00.02.DH0‡	1-16
	1.00.04.DH0‡	3-16
	1.00.05.DH0	3-6, 8-16
	1.00.06.DH0	3-6, 8-16
	1.00.07.DH0	3, 5-6, 8-12, 16
659122-602	1.00.01.DH0‡	1-16
	1.00.02.DH0‡	1-16
	1.00.04.DH0‡	3-16
	1.00.05.DH0	3-6, 8-16
	1.00.06.DH0	3-6, 8-16
	1.00.07.DH0	3, 5-6, 8-12, 16
659122-603	1.00.01.DH0‡	1-16
	1.00.02.DH0‡	1-16
	1.00.04.DH0‡	3-16
	1.00.05.DH0	3-6, 8-16
	1.00.06.DH0	3-6, 8-16
	1.00.07.DH0	3, 5-6, 8-12, 16
663350-502	1.00.01.DH0‡	1-16
	1.00.02.DH0‡	1-16
	1.00.04.DH0	3-16
	1.00.05.DH0	3-6, 8-16
	1.00.06.DH0	3-6, 8-16
	1.00.07.DH0	3, 5-6, 8-12, 16
663350-503	1.00.01.DH0‡	1-16
	1.00.02.DH0‡	1-16
	1.00.04.DH0	3-16
	1.00.05.DH0	3-6, 8-16
	1.00.06.DH0	3-6, 8-16
	1.00.07.DH0	3, 5-6, 8-12, 16

PBA Revision	BIOS Revision	Errata That Apply
663350-504	1.00.01.DH0‡	1-16
	1.00.02.DH0‡	1-16
	1.00.04.DH0‡	3-16
	1.00.05.DH0	3-6, 8-16
	1.00.06.DH0	3-6, 8-16
	1.00.07.DH0	3, 5-6, 8-12, 16
663350-602	1.00.01.DH0‡	1-16
	1.00.02.DH0‡	1-16
	1.00.04.DH0‡	3-16
	1.00.05.DH0	3-6, 8-16
	1.00.06.DH0	3-6, 8-16
	1.00.07.DH0	3, 5-6, 8-12, 16
663350-603	1.00.01.DH0‡	1-16
	1.00.02.DH0‡	1-16
	1.00.04.DH0‡	3-16
	1.00.05.DH0	3-6, 8-16
	1.00.06.DH0	3-6, 8-16
	1.00.07.DH0	3, 5-6, 8-12, 16
666736-601	1.00.01.DH0‡	1-16
	1.00.02.DH0‡	1-16
	1.00.04.DH0‡	3-16
	1.00.05.DH0	3-6, 8-16
	1.00.06.DH0	3-6, 8-16
	1.00.07.DH0	3, 5-6, 8-12, 16
666736-602	1.00.01.DH0‡	1-16
	1.00.02.DH0‡	1-16
	1.00.04.DH0‡	3-16
	1.00.05.DH0	3-6, 8-16
	1.00.06.DH0	3-6, 8-16
	1.00.07.DH0	3, 5-6, 8-12, 16

PBA Revision	BIOS Revision	Errata That Apply
666737-601	1.00.01.DH0‡	1-16
	1.00.02.DH0‡	1-16
	1.00.04.DH0‡	3-16
	1.00.05.DH0	3-6, 8-16
	1.00.06.DH0	3-6, 8-16
	1.00.07.DH0	3, 5-6, 8-12, 16
666737-602	1.00.01.DH0‡	1-16
	1.00.02.DH0‡	1-16
	1.00.04.DH0‡	3-16
	1.00.05.DH0	3-6, 8-16
	1.00.06.DH0	3-6, 8-16
	1.00.07.DH0	3, 5-6, 8-12, 16
666737-603	1.00.01.DH0‡	1-16
	1.00.02.DH0‡	1-16
	1.00.04.DH0‡	3-16
	1.00.05.DH0‡	3-6, 8-16
	1.00.06.DH0	3-6, 8-16
	1.00.07.DH0	3, 5-6, 8-12, 16
668221-601	1.00.01.DH0‡	1-16
	1.00.02.DH0‡	1-16
	1.00.04.DH0‡	3-16
	1.00.05.DH0	3-6, 8-16
	1.00.06.DH0	3-6, 8-16
	1.00.07.DH0	3, 5-6, 8-12, 16
668221-602	1.00.01.DH0‡	1-16
	1.00.02.DH0‡	1-16
	1.00.04.DH0‡	3-16
	1.00.05.DH0	3-6, 8-16
	1.00.06.DH0	3-6, 8-16
	1.00.07.DH0	3, 5-6, 8-12, 16

PBA Revision	BIOS Revision	Errata That Apply
677266-602	1.00.01.DH0‡	1-16
	1.00.02.DH0‡	1-16
	1.00.04.DH0‡	3-16
	1.00.05.DH0	3-6, 8-16
	1.00.06.DH0	3-6, 8-16
	1.00.07.DH0	3, 5-6, 8-12, 16
677266-603	1.00.01.DH0‡	1-16
	1.00.02.DH0‡	1-16
	1.00.04.DH0‡	3-16
	1.00.05.DH0	3-6, 8-16
	1.00.06.DH0	3-6, 8-16
	1.00.07.DH0	3, 5-6, 8-12, 16
677266-604	1.00.01.DH0‡	1-16
	1.00.02.DH0‡	1-16
	1.00.04.DH0‡	3-16
	1.00.05.DH0	3-6, 8-16
	1.00.06.DH0	3-6, 8-16
	1.00.07.DH0	3, 5-6, 8-12, 16
677267-603	1.00.01.DH0‡	1-16
	1.00.02.DH0‡	1-16
	1.00.04.DH0‡	3-16
	1.00.05.DH0‡	3-6, 8-16
	1.00.06.DH0	3-6, 8-16
	1.00.07.DH0	3, 5-6, 8-12, 16
677267-604	1.00.01.DH0‡	1-16
	1.00.02.DH0‡	1-16
	1.00.04.DH0‡	3-16
	1.00.05.DH0‡	3-6, 8-16
	1.00.06.DH0	3-6, 8-16
	1.00.07.DH0	3, 5-6, 8-12, 16

PBA Revision	BIOS Revision	Errata That Apply
677267-605	1.00.01.DH0‡	1-16
	1.00.02.DH0‡	1-16
	1.00.04.DH0‡	3-16
	1.00.05.DH0‡	3-6, 8-16
	1.00.06.DH0	3-6, 8-16
	1.00.07.DH0	3, 5-6, 8-12, 16

NOTE:

‡   This combination of BIOS revision and PBA revision has not undergone regression testing. Use of a PBA with down-revision BIOS is an untested combination and is undertaken at the user's risk.

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SPECIFICATION CHANGES

The Specification Changes listed in this section apply to the *TC430HX Motherboard Technical Product Specification* (Order Number 281820). All Specification Changes will be incorporated into a future version of that specification.

1. *Support for 233 MHz Pentium® processors with MMX™ technology*

Support for 233 MHz Pentium® processors with MMX™ technology is available in PBA revision 677266-602, 677267-603 and higher. Below are the jumper settings:

Microprocessor Freq. (MHz)	Host Bus Freq. (MHz)	Jumper Settings for J10C1-C	Jumper Settings for J10C1-D	PCI Freq. (MHz)	Clock Ratio	ISA Freq. (MHz)
100/233	66	1-2 and 5-6	1-2 and 4-5	33	3/2	8.33

NOTE:

There are no additional jumpering requirements for Pentium processors with MMX technology.

The 100 MHz Pentium processor and the 233 MHz Pentium processor with MMX technology have identical jumper settings. The motherboard automatically detects which processor type is installed.

2. *User Password Clear Feature*

A user password clear feature has been added to allow an administrator to clear the user password in the BIOS Setup Security screen. The option for the Administrator to clear the user password is only available in BIOS Revision 1.00.07.DH0 and higher. See Documentation Change 7 for further information.

3. *LS-120 Drive Support*

Support for the LS-120 drive has been added and the following text will be added as Section 1.6.4.1:

LS-120 MB Diskette technology enables users to store 120 MB of data on a single, 3.5-inch removable diskette. LS-120 technology is backward (both read and write) compatible with 1.44 MB and 720 KB DOS-formatted diskettes and is supported by Windows* 95 and Windows NT* operating systems.

The TC430HX motherboard allows connection of an LS-120 compatible drive and a standard 3.5-inch diskette drive. The LS-120 drive can be configured as a boot device, if selected as a floppy device in the BIOS setup utility.

⟹ **NOTE**

If you connect an LS-120 drive to an IDE connector and configure it as the "A" drive and configure a standard 3.5-inch floppy as a "B" drive, the standard floppy must be connected to the floppy drive cable's "A" connector (the connector at the end of the cable).

ERRATA

1. ECC Non-detection of Single/Double Bit Errors on Partial Memory Writes

PROBLEM: When the 82439HX TXC performs a partial write to main memory (data less than a 64-bit quadword) in ECC mode, single bit errors are corrected but not logged. Double bit errors are not detected or logged.

IMPLICATION: Normally, the controller is able to buffer writes and group them into quadwords. In all these cases where 64 bits are written to memory at a time, both single and double bit errors will be signaled to the operating system. Single bit errors will be corrected using the information contained in the checkbits that are stored with the data in memory. Double bit errors cannot be corrected by the memory controller, but the operating system can warn the user that the error has occurred.

If the controller must perform a partial write, a read-merge-write cycle will occur so that the proper checkbits can be regenerated across the entire 64 bits to be written into DRAM. If erroneous data is read during this cycle, the following will occur:

For single bit errors, the error will be corrected based on the memory checkbits. The corrected data will be written back to memory, but the error will not be flagged to the system, so the user will not receive information from the error log that could be useful in isolating a failing memory module.

For double-bit errors, no error will be detected or signaled to the operating system. The erroneous data will be rewritten to memory and a set of regenerated checkbits will be rewritten at the same time, marking the erroneous data as correct.

WORKAROUND: None. However, for ECC systems that require only single bit error protection, the A1 stepping of the 430HX PCIset does provide this level of reliability.

STATUS: This erratum was fixed in PBA revision 659122-503 and 663350-502 when using BIOS revision 1.00.04.DH0.

2. PCI Delayed Transactions Are Not Supported

PROBLEM: An erratum to the A1 stepping of the 82371SB PCI ISA IDE Xcelerator (PIIX3) requires that the option for Delayed Transactions be turned off by the BIOS.

IMPLICATION: System level performance and compatibility are not affected by turning off delayed transactions. The system will be PCI 2.1 compatible and will support all PCI 2.1 compliant cards.

WORKAROUND: None.

STATUS: This erratum was fixed in PBA revision 659122-503 and 663350-502 when using BIOS revision 1.00.04.DH0.

3. MIDI to WAV Recording May Result in Distortion on Playback

PROBLEM: Recording a MIDI to WAV file in Microsoft Windows* 95 using the Media Player and Sound Recorder applications causes distortion in the recorded playback if the gain for the volume control and synthesizer is set greater than 50 percent.

IMPLICATION: During playback of a WAV file audio distortion will be heard if the recording was done with greater than 50 percent gain.

WORKAROUND: Keep the volume control and synthesizer gain settings at less than 50 percent levels. Mute all mixers in the volume control window except volume control and synthesizer.

STATUS: This erratum will be fixed in a future release of the Yamaha audio drivers.

4. BIOS Does Not Support No-Emulation Mode for CD-ROM Boot

PROBLEM: The system BIOS does not support booting from an "El Torito" bootable CD-ROM using the no-emulation mode format.

IMPLICATION: Booting from a CD-ROM using no emulation mode is not supported. For example, Microsoft Windows* NT* version 4.0 uses no-emulation mode for its boot CD-ROM.

WORKAROUND: Boot the computer from a floppy or hard disk, then install or run the program from the CD-ROM.

STATUS: This erratum was fixed in BIOS revision 1.00.07.DH0.

5. System BIOS Does Not Recognize Bootable USB Devices

PROBLEM: The system BIOS does not recognize a USB keyboard or mouse during a system boot. A USB keyboard or mouse is not recognized until an operating system that supports USB is loaded.

IMPLICATION: 1. The user is not able to use a USB keyboard to enter the BIOS Setup or to respond to error messages that are displayed before an operating system with USB support is loaded.
2. The user is not able to use a USB keyboard or mouse with any operating system that does not have USB support.

WORKAROUND: Use a standard PS/2* style keyboard and mouse in any configuration where input is required before an operating system with USB support is loaded.

STATUS: This erratum will be fixed in a future BIOS revision.

6. USB Voltage May Drop Below 4.75 Volts

PROBLEM: The actual voltage at the motherboard USB connectors may drop below the 4.75 volt minimum requirement in USB Specification 1.0 when a USB device is attached to the motherboard. The TC430HX Motherboard Technical Product Specification (281820-001) states that a 5 volt power supply with a +/- 5% tolerance is required meaning that 4.75 volts would be worst case. A power supply producing a worst case 4.75 volts at the motherboard power connector will result in less than 4.75 volts available at the motherboard USB connectors due to the effective series resistance between the power supply and the USB connectors.

IMPLICATION: A USB device that is sensitive to an under voltage condition may not respond as expected when attached to the motherboard USB connector.

WORKAROUND: None.

STATUS: This erratum will not be fixed.

7. CMOS Checksum May Be Lost If Power Is Cycled During Boot

PROBLEM: If the computer power is turned off during a short portion of the boot process, the CMOS checksum byte is not updated. The next time the computer is turned on, the message "CMOS Checksum Invalid" will be displayed.

IMPLICATION: When the message is displayed, the correct checksum has already been recalculated and stored. No user action is required to recover from the error. If the additional message:

> Date and Time Not Set
> Press <F1> for Setup, <Esc> to Boot

is displayed, the user must reset the current date and time using the BIOS Setup program.

WORKAROUND: None.

STATUS: This erratum was fixed in BIOS revision 1.00.05.DH0.

8. PCI Device Scan May Terminate Abnormally

PROBLEM: If the system does not contain a device with PCI ID Bus 00, Device 07, Function 3, any program that polls for PCI devices will receive a partial response at that address. If the program is not able to recover from that partial response it may cause the computer to lock up.

IMPLICATION: The user may have to reboot the computer after running a PCI diagnostic program. This is only known to affect the proprietary PCI diagnostic program PCI.EXE. Intel does not know of any application program subject to this erratum.

WORKAROUND: None.

STATUS: This erratum will not be fixed.

9. PCI Add-in Card May Hang System Due to Improper TRST# Signal

PROBLEM: If a PCI add-in card that implements boundary scan is installed, the system may not boot. In accordance with the PCI 2.1 specification, the add-in card expects the TRST# signal to be pulled down if JTAG is not supported by the motherboard. The motherboard does not implement JTAG boundary scan and does not pull the TRST# signal down, which prevents the add-in card from initializing properly.

IMPLICATION: The system may not boot if a PCI card that implements JTAG boundary scan is inserted.

WORKAROUND: None.

STATUS: This erratum will not be fixed.

10. Slave on Secondary IDE Channel Is Not Disabled

PROBLEM: If the IDE Device Configuration option in BIOS Setup is set to disable the secondary IDE slave device, it will not be disabled in the following configuration:

- ATAPI device attached as master to the secondary IDE connector.

- ATAPI device attached as slave to the secondary IDE connector.

IMPLICATION: In the above configuration, any ATAPI device attached as a secondary slave will remain enabled even if the BIOS setting for the secondary slave is set to disabled.

WORKAROUND: None.

STATUS: This erratum will not be fixed.

11. Cannot Meet FCC Class B Requirements using Unshielded USB Cable

PROBLEM: The motherboard will generate excessive electromagnetic radiation on unshielded USB cables, even if no device or a low speed (sub-channel) USB device is attached to the cable.

IMPLICATION: Systems based on this motherboard will not meet FCC Part 15 Class B requirements when unshielded USB cable is used. Although this condition is a violation of the USB v1.0 specification, it is not believed to have any effect on normal USB device operation.

WORKAROUND: Use USB devices with shielded cable that meet the requirements for high speed (fully-rated) USB devices.

STATUS: This erratum will not be fixed.

12. Audio Driver Does Not Support Windows* 3.x Session Within OS/2* Warp*

PROBLEM: The TC430HX motherboard audio drivers for OS/2* Warp* or Windows* 3.x do not support audio during a Windows 3.x session within OS/2 Warp.

IMPLICATION: No audio is available during a Windows 3.x session within OS/2 Warp. Normal audio support will be available in native OS/2 Warp.

WORKAROUND: None.

STATUS: This erratum will not be fixed.

13. System BIOS Does Not Allocate IRQ Resources to PCI Video Cards

PROBLEM: An interrupt is not allocated to a PCI video card when the system boots.

IMPLICATION: The video card's enhanced features may not be available in some software applications.

WORKAROUND: None.

STATUS: This erratum was fixed in BIOS revision 1.00.07.DH0.

14. System BIOS May Assign Conflicting Resources for Parallel Port

PROBLEM: If the PnP Configuration is set to Use Setup and IRQ 7 is set to Used by ISA Device in BIOS Setup, it is possible to enable the parallel port in the Peripheral Configuration menu to use IRQ 7.

IMPLICATION: The system will report a device conflict on boot.

WORKAROUND: None.

STATUS: This erratum was fixed in BIOS revision 1.00.07.DH0.

15.   System BIOS May Corrupt Audio Add-In Card EEPROM

PROBLEM: Audio add-in cards using the Yamaha OPL3-SA2 or OPL3-SA3 audio codec have the same hardware identification number that is used by the Yamaha audio device integrated on the motherboard. This causes the system BIOS to inadvertently write information into the audio add-in card's serial EEPROM during system startup, thereby corrupting the audio add-in card's EEPROM contents.

IMPLICATION: The audio add-in card will not operate and no audio will be available.

WORKAROUND: Disable the onboard audio in BIOS Setup before installing an audio add-in card.

STATUS: This erratum will not be fixed.

16.   MIDI Playback Not Available in OS/2* Warp* 3.0

PROBLEM: The MIDI player in OS/2* Warp* 3.0 loads and behaves as though it is working, however, the progression indicator will not move and no MIDI audio will be heard.

IMPLICATION: MIDI playback will not be available if the integrated wavetable device is on the motherboard.

WORKAROUND: None.

STATUS: This erratum was fixed in release 3.02 of the Yamaha audio drivers.

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SPECIFICATION CLARIFICATIONS

The Specification Clarifications listed in this section apply to the *TC430HX Motherboard Technical Product Specification* (Order Number 281820). All Specification Clarifications will be incorporated into a future version of that specification.

1.   *Advanced Power Management (APM) Will Not Function as Expected with Universal Serial Bus (USB) Enabled*

The following will be added to Section 1.6.3, Universal Serial Bus and Section 3.7, Advanced Power Management:

Advanced Power Management will not function as expected when a USB keyboard or mouse is used. USB activity is not monitored by the APM event counter, therefore, activity from a USB keyboard or mouse will not keep the system awake or bring a system out of APM sleep mode. If a USB keyboard or mouse is being used, APM should be disabled.

2.   *PCI 2.1 Specification Optional Features*

The following will be added to section 1.10.10, PCI Connectors - J4C1, J4D1, J4D2, J4E1:

The following optional features in the PCI 2.1 Specification are not implemented on the TC430HX motherboard:

- Cache Support Pins **SBO#** and **SDONE** (Section 2.2.7)
- **PRSNTx#** (Section 2.2.8)
- **CLKRUN#** (Section 2.2.8)
- 64 Bit Bus Extension Pins (Section 2.2.9)
- 66 MHz support (Section 2.2.8)
- JTAG/Boundary scan (Section 2.2.10)

3.   *Power Supply Considerations*

The TC430HX motherboard has been designed to be configured in a system that uses a power supply that complies with the recommendations of ATX Specification Version 2.01. See Documentation Change 11 for the specific recommendations that must be met by a power supply for the motherboard.

DOCUMENTATION CHANGES

The Documentation Changes listed in this section apply to the *TC430HX Motherboard Technical Product Specification* (Order Number 281820). All Documentation Changes will be incorporated into a future version of the appropriate TC430HX motherboard documentation.

1.   Revision of Section 1.10.12.1, Speaker

This section will be replaced in its entirety as follows:

The PC speaker provides error beep code information during the Power-On Self Test. However, stereo audio requires that external speakers be plugged into the audio output.

2.   Revision of Section 1.2, Motherboard Manufacturing Options

The following will be added to the end of this section:

If the onboard S3* ViRGE* or ViRGE/DX* graphics controller is installed, the shared PCI slot (J4C1) will not be populated.

3.   Revision of Section 1.10.13.2, Wavetable Upgrade

This second paragraph in this section will be replaced in its entirety as follows:

Compatible wavetable cards are available from several vendors.

4.   Revision of Section 1.6.1, 82439HX Xcelerated Controller (TXC)

The fourth bullet in this section will be replaced in its entirety as follows:

- Fully synchronous PCI bus interface

    — 25/30/33 MHz

    — PCI to DRAM data transfers up to or greater than 100 MB/sec

    — Up to 4 PCI masters in addition to the PIIX3

5.   Revision of Section 1.10.10, PCI Connectors - J4C1, J4D1, J4D2, J4E1

The following text will be added to the beginning of this section:

The motherboard Expansion Slots support up to four bus mastering PCI add-in boards. One of the PCI slots may be shared with an ISA slot.

6.   Addition of Onboard Video IRQ Section

The following section will be added after Section 3.12.9.8:

ONBOARD VIDEO IRQ

Enables or disables the allocation of an interrupt to the onboard video controller. The options are:

- Disabled
- Enabled (**default**)

7.   *Revision of Section 3.12.12, Security Screen*

This section will be replaced in its entirety as follows:

This section describes the options that can be set to restrict access to the Setup program and to restrict who can boot the computer.

An administrative password and a user password can be set for the Setup program and for booting the computer, with the following restrictions:

- The administrative password gives unrestricted access to view and change all the Setup options in the Setup program. This is administrative mode.

- The user password gives restricted access to view and change Setup options in the Setup program. This is user mode. The level of user-mode access is set with the User Privilege Level option. See Section 0 for information about the User Privilege Level option.

- If only the administrative password is set, pressing the <Enter> key at the password prompt of the Setup program allows the user restricted access to Setup. The restricted access is the level set for the User Privilege Level option.

- If both the administrative and user passwords are set, users can enter either the administrative password or the user password to access Setup. Users have access to Setup respective to which password is entered.

- Setting the user password restricts who can boot the computer. The password prompt will be displayed before the computer is booted. If only the administrative password is set, the computer boots without asking for a password. If both passwords are set, the user can enter either password to boot the computer.

Table 16 shows the effects of setting the administrative password and user password. This table is for reference only and is not displayed on the screen.

Table 16.   Administrative and User Password Functions

Password Set	Administrative Mode	User Mode	Setup Options	Password to Enter Setup	Password During Boot
Neither	Can change all options *	Can change all options *	None	None	None
Administrative only	Can change all options	Can change a limited number of options **	Administrative Password User Privilege Level	Administrative	None
User only	N/A	Can change all options	Enter Password Clear User Password	User	User
Administrative and user set	Can change all options	Can change a limited number of options **	Administrative Password User Privilege Level Enter Password	Administrative or user	Administrative or user

*   If no password is set, any user can change all Setup options.

**   The level of user access is set with the User Privilege Level option. See Section 0 for more information about the User Privilege Level option.

USER PASSWORD

Reports if there is a user password set. There are no options.

ADMINISTRATIVE PASSWORD

Reports if there is an administrative password set. There are no options.

ENTER PASSWORD

Sets the user password. The password can be up to seven alphanumeric characters.

SET ADMINISTRATIVE PASSWORD

Sets the administrative password. The password can be up to seven alphanumeric characters.

USER PRIVILEGE LEVEL

Sets the level of access users can have to the Setup program. This option can be set only by an administrative user with access to the administrative password. This option is displayed only when an administrative password is set. The options are:

- Limited Access **(default)**
- No access
- View Only
- Full Access

The following table specifies the permitted access to Setup for each option:

Table 17.   Access for User Privilege Level Options

Option	Access
Limited Access	User can access the Setup program and can change the following options: System Date, System Time, User Password, Unattended Start, and Security Hot-Key. Other Setup options are not visible.
No access	User cannot access the Setup program.
View Only	User can access the Setup program and view options, but cannot change any options.
Full Access	User can access the Setup program and can change all options except User Privilege Level and Set Administrative Password.

CLEAR USER PASSWORD

Clears the current user password. The user password must be set to enable this field.

UNATTENDED START

Controls when the security password is requested. The user password must be set to enable this field. The options are:

- Enabled (the system boots, but the keyboard is locked until the user password is entered)

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• Disabled (the system does not boot until the user password is entered) **(default)**

SECURITY HOT KEY (CTRL-ALT-)

Sets a hot key that locks the keyboard until the user password is entered. All alphabetic keys are valid entries for this field. When a user presses this key while holding down the <Ctrl> and <Alt> keys, the keyboard locks and the keyboard LEDs flash to indicate that the keyboard is locked.

➡ **NOTE**

> *If the user sets the Security hot key and the APM hot key (see Section 3.12.10.5) to the same key,*
>
> *the APM function has priority.*

8. Revision of Section 3.12.3.3, Floppy A: Type

The following will be added as the last option to this section for LS-120 drive support:

120 MB, 3.5-inch

9. Revision of Section 3.12.3.4, Floppy B: Type

The following will be added as the last option to this section for LS-120 drive support:

120 MB, 3.5-inch

10. Revision of Section 1.11.3, Clear CMOS (J10C1-A, Pins 4, 5 and 6)

This section will be replaced in its entirety as follows:

Allows CMOS settings to be reset to default values by moving the jumper from pins 4-5 to pins 5-6 and turning the system on. When the system reports that "NVRAM cleared by jumper", the system can be turned off, and the jumper should be returned to the 4-5 position to restore normal operation. Default is for this jumper to be on pins 4-5.

Caution: This procedure should only be done if, after a BIOS update, the system does not boot to a point where BIOS Setup can be entered or if, after CMOS default settings have been restored from within the Setup program, the system does not boot to the operating system.

11. Addition of Power Supply Considerations Section

The following section will be added between 1.14 and 1.15. All corresponding sections will be renumbered as appropriate.

For typical configurations, the motherboard is designed to operate with at least a 200 W power supply that complies with version 2.01 of the ATX Specification. A higher-wattage power supply should be used for heavily-loaded configurations. The power supply must comply with the following recommendations found in the indicated sections of that specification:

• The potential relation between 3.3VDC and +5VDC power rails (Section 4.2)
• The current capability of the +5VSB line (Section 4.2.1.2)

- All timing parameters (Section 4.2.1.3)
- All voltage tolerances (Section 4.2.2)

12. *Revision of Section 1.9, Audio Subsystem*

The following note will be added to this section:

⟹ **NOTE**

The audio subsystem requires an unbalanced microphone, either electret or dynamic with an output voltage level of 30 mv to 200 mv. The impedance range should be 200 ohms to 2000 ohms.

13. *Revision of Section 1.10.14.3, Serial Port Connector*

The section will be replaced in its entirety as follows:

Pin	Signal Name
1	DCD
2	Serial In#
3	Serial Out#
4	DTR#
5	Ground
6	DSR#
7	RTS#
8	CTS#
9	Ring Indicator#

14. *Revision of Section 1.11.1, Microprocessor Configuration (J10C1-C, D)*

The section will be replaced in its entirety as follows:

These allow the board to be switched between different speeds of the processor. These jumpers also affect the PCI and ISA clock speeds according to the following table.

Table 6.   Microprocessor/Bus Speed Settings

Microprocessor Freq. (MHz)	Host Bus Freq. (MHz)	Jumper Settings for J10C1-C	Jumper Settings for J10C1-D	PCI Freq. (MHz)	Clock Ratio	ISA Freq. (MHz)
100/233	66	1-2 and 5-6	1-2 and 4-5	33	3/2	8.33
200	66	1-2 and 5-6	1-2 and 5-6	33	6/2	8.33
166	66	1-2 and 5-6	2-3 and 5-6	33	5/2	8.33
150	60	2-3 and 4-5	2-3 and 5-6	30	5/2	7.5
133	66	1-2 and 5-6	2-3 and 4-5	33	4/2	8.33
120	60	2-3 and 4-5	2-3 and 4-5	30	4/2	7.5
100	66	1-2 and 5-6	1-2 and 4-5	33	3/2	8.33
90	60	2-3 and 4-5	1-2 and 4-5	30	3/2	7.5
75	50	2-3 and 5-6	1-2 and 4-5	25	3/2	8.33

⟹ **NOTE**

Pins 1 and 4 are not present in jumper block J10C1-D on some versions of the TC430HX motherboard. Where a pin listed above in the settings for J10C1-D is not present, no jumper needs to be installed.

There are no separate or additional jumpering requirements needed to support the 2.8 voltage requirements for Pentium processors with MMX technology.

The 100 MHz Pentium processor and the 233 MHz Pentium processor with MMX technology have identical jumper settings. The motherboard automatically detects which processor type is installed.