SE7500CW2 Server Board SC5200 Server Chassis

Specification Update

Intel Order Number C19123-001



January, 2003

Enterprise Platforms and Services Marketing

Revision History

Date	Modifications
September, 2002	Initial release.
October, 2002	Added details on NetWare 6.0 SP2 installation, Intel® LANDesk Client Manager 6.3 Wake on LAN limitation, Shock and Vibe data, and several miscellaneous issues.
November, 2002	Added update on Promise* ATA working with hard-drives larger than 137GB, and more Adaptec* RAID adapter information.
December, 2002	Added two brief documentation changes, update Intel® LANDesk Client Manger 6.3, added new item on BIOS.
January, 2003	Added information on BIOS POST for logical processors, 4314 Beep code, and UUID.

Disclaimers

The SE7500CW2 Server Board, and SC5200 Server Chassis may contain design defects or errors known as errata that may cause the product to deviate from the published specifications. Current characterized errata are documented in this Specification Update.

Information in this document is provided in connection with Intel products. No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document. Except as provided in Intel's Terms and Conditions of Sale for such products, Intel assumes no liability whatsoever, and Intel disclaims any express or implied warranty, relating to sale and/or use of Intel products including liability or warranties relating to fitness for a particular purpose, merchantability, or infringement of any patent, copyright or other intellectual property right. Intel products are not intended for use in medical, life saving, or life sustaining applications. Intel may make changes to specifications and product descriptions at any time, without notice.

Contact your local Intel sales office or your distributor to obtain the latest specifications and before placing your product order.

Intel, Itanium, Pentium, and Xeon are trademarks or registered trademarks of Intel Corporation.

*Other brands and names may be claimed as the property of others.

Copyright © Intel Corporation 2003.

Contents

Preface	1
Summary Tables of Changes	3
	_
rrata	5

This page intentionally left blank

Preface

This document is an update to the product definition specified in the *SE7500CW2 Server Board Technical Product Specification* (Order Number A19122-001), and SC5200 Technical Product Specification (Order Number A99108-001). It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools. It will contain specification changes, specification clarifications, errata, and document changes.

Refer to the *Intel® Xeon™ Processor Specification Update* for specification updates concerning the Intel® Xeon™ processor. *Items contained in the Intel® Processor Specification Update* that either do not apply to the SE7500CW2 Server board or have been worked around is noted in this document. Otherwise, it should be assumed that any processor errata for a given stepping are applicable to the Printed Board Assembly (PBA) revisions(s) associated with that stepping.

Nomenclature

- **Specification Changes** are modifications to the current published specifications for the SE7500CW2 server board, and SC5200 Server Chassis. These changes will be incorporated in a future release of the given document.
- **Specification Clarifications** describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in a future release of the given document.
- Documentation Changes include typos, errors, or omissions from documents that are currently published. These documents may include Product Specs and Users Guides. These changes will be incorporated in a future release of the given document.
- **Errata** are design defects or errors. Errata may cause operation of a specified product to deviate from published specifications. Hardware and software designed to be used with any given processor stepping must assume that all errata documented for that processor stepping are present on all devices. Errata listed in this document that have no plans to be fixed will be listed in later revisions of current published specifications for the given product.

Product Scope

Below are the specific SE7500CW2 board revisions covered in this document.

Product Code	Order Code	Top Assembly #	Baseboard PBA #	BIOS Rev./	HSC Revision	Product Change
	(MM#)	(TA#)	. 2	Build#		Notification #
BCWBB	845413	A88031-502	A87967-502	1.10	.09	(1 st Production)
SE7500CW2	845398	A88029-001	A87967-502			
BCWBB	845413	A88031-503	A87967-503	1.10	.09	N/A
SE7500CW2	845398	A88029-001	A87967-503			
SE7500CW2SCSI	845399	A88030-001	A87967-503			
BCWBB	845413	A88031-504	A87967-504	1.10	.09	PCN
SE7500CW2	845398	A88029-002	A87967-504			102650-00
SE7500CW2SCSI	845399	A88030-001	A87967-504			
BCWBB	849161	A88031-505	A87967-505	1.12	.09	PCN
SE7500CW2	845398	A88029-003	A87967-505			102580-01
SE7500CW2SCSI	845399	A88030-002	A87967-505			
BCWBB	851384	A88031-505	A87967-506	1.17	.10	PCN
SE7500CW2	845398	A88029-004	A87967-506			102815-01
SE7500CW2SCSI	845399	A88030-003	A87967-506			
BCWBB	TBD	A88031-506	A87967-507	1.23	.11	PCN
SE7500CW2	845398	A88029-006	A87967-507			103036-01
SE7500CW2SCSI	845399	A88030-005	A87967-507			

Below are the specific SC5200 chassis revisions covered in this document.

Product Code	Order Code (MM #)	Top Assembly # (TA #)	Front Panel PBA#	HSC Firmware Rev.	Power Supply Module Part #	Product Change Notification #
KHD3BASE450	844923	A85319-001	835851	NA	844924	NA 1 st Production
KHD3BASE450	844923	A85319-002	835851	NA	844924	PCN 102640-01

Summary Tables of Changes

The following tables indicate the errata and the document changes that apply to the SE7500CW2 Server Board. Intel intends to fix some of the specified errata in future updates to the server board. Documentation changes will be made in future updates to the given document. The tables use the following notations:

Doc: Intel intends to update the appropriate document in a future revision.

Investigating Intel is investigating the issue.

Fix: Intel intends to fix this erratum in a future update of the board.

Fixed: This erratum has been addressed.

NoFix: There are no plans to fix this erratum.

Shaded: This erratum is either new or has been modified from the previous

specification update.

Table 1. Errata Summary

No.	Plans	Description of Errata
1.	Fixed	Intel® Xeon processors 2.6 GHz and 2.8 GHz C1 stepping not supported in BIOS 1.14.
2.	Fixed	LDCM 6.3 reported processor speeds change after a system reboot.
3.	Fixed	I can't get my Adaptec 2100S RAID card to clear POST.
4.	Fixed	NetWare 6.0 Service Pack 2 won't install with Hyper-threading enabled in BIOS.
5.	NoFix	Disabling PXE support in BIOS doesn't correctly disable Network boot support with a PCI NIC add-in card.
6.	NoFix	BIOS is unable to select IDE CD-ROM or USB CDROM as a boot device.
7.	Investigating	LDCM 6.3 build 211 Wake on LAN does not reboot the server.
8.	Investigating	Windows 2000* won't install on a Maxtor D540X-4G 137GIG ATA hard-drive.
9.	Investigating	Adaptec 2100S, 2110S, and 3410S, RAID cards cause LILO to hang with Red Hat 7.3.
10.	Investigating	LDCM 6.3 build 211 incorrectly lowers processor fan speed.
11.	Fixed	BIOS EBDA area disabled in BIOS 1.17.
12.	Investigating	Disable NIC in BIOS incorrectly disables incorrect NIC number.
13.	Investigating	UUID not programmed on all PBA # A87967-506 and older boards.
14.	Fixed	Logical processors not listed in BIOS POST if hyper-threading is enabled in F2 BIOS setup.

Table 2. Documentation Changes

No.	Plans	Description of Documentation Change
1.	Fix in Future TPS release	Shock and Vibe test results aren't described in the TPS.
2.	Fix in Future TPS Release	The TPS doesn't contain information on the LED pin-out for the bundled Intel® 53C1000B1 SCSI card.
3.	Fix in Future TPS Release	The TPS doesn't explain how BIOS automatically disables the onboard video if a video add-in card is added.
4.	Fix in Future TPS Release	BIOS beep code 4-3-1-4 not mentioned in the TPS.

Following are in-depth descriptions of each erratum / documentation change indicated in the tables above. The errata and documentation change numbers below correspond to the numbers in the tables.

Errata

1. Intel® Xeon processors 2.6 GHz and 2.8 GHz C1 stepping not supported in BIOS

1.14.	stepping not supported in Bioc
1.14.	
Problem	The SE7500CW2 BIOS 1.14 does not support Intel® Xeon
	processors running at 2.6 Ghz, and 2.8 GHz.
Implication	Intel® Xeon processors running at 2.6GHz and 2.8GHz won't
	boot with the currently supported production BIOS 1.14. In
	other words, this BIOS doesn't support the C1 stepping that is
	required by these processors.
Workaround	None.
Status	These processor speeds are now supported with BIOS 1.16 and above.
	Please check http://support.intel.com download details.

2. Intel® LANDesk Client Manger (LDCM) 6.3 reports different processor speeds after a rebooting Windows* 2000

Problem Intel® Xeon processor speeds change in the LDCM 6.3 after a reboot.

Implication The speed that LDCM reports may be incorrect, and change

after a reboot. Also, the speed may be slightly slower or faster

than actual processor speed.

Workaround Use the processor speed listed in BIOS <F2> setup under the

"System – CPU" sub-menu.

Status Intel is investigating the possiblity of fixing this erratum.

3. My SE7500CW2 system won't boot to DOS with an Adaptec* card installed.

Problem SE7500CW2 system boots to the Adaptec SMOR utility

instead of booting into DOS.

Implication When running the Adaptec card in "EBDA relocation" mode

the system will not boot. If Adaptec's card "EBDA Relocation"

mode is disabled on SE7500CW2 BIOS 1.12 the card will

perform correctly under some circumstances.

Workaround Create boot disks using Windows 98 DOS instead of DOS 6.22 or the

ROM-DOS shipped on the resource CD.

Status This issue is resolved with a new release of the Adaptec BIOS and

SE7500CW2 BIOS 1.16. The Adaptec BIOS v1.30 should work

correctly. BIOS 1.16 and 1.17 are now available for the

SE7500CW2. Both should work properly with this card.

4. NetWare Service Pack 2 won't allow BIOS to enable hyper-threading functionality.

Problem The acpidrv.psm and scpica.nlm files included support pack 2

don't allow for hyper-threading enabling in BIOS v1.17 and below.

The PSM fails to load with the following error: "GPEO block

overlaps the GPE1 block. Error initializing the ACPI system."

Implication

Processor performance of some applications will be hindered

without hyper-threading support. Hence, NetWare 6.0 will only

be able to use one virtual processor.

Workaround

The workaround is to use NetWare 6.0 Service Pack 1 if the

hyper-threading performance enhancement is required. The

ACPI functionality in this service pack works correctly.

Status This has been fixed in BIOS 1.18.

5. Disabling PXE support in BIOS doesn't correctly disable Network boot support with a PCI NIC add-in card.

Problem After setting BIOS <F2> setup "Advanced" sub-menu's "PXE Support" to

disabled and rebooting, the <F2> boot menu still incorrectly displays the

"Network Boot" as a boot option. The "Boot" menu then incorrectly

displays the "Network Boot" device as "Intel UNDI, PXE-1.0 (Build Dev)."

Implication

Users may incorrectly expect that the "Network" boot is still available

since it is listed in the <F2> setup "Boot" sub-menu.

Workaround

None

Status

No fix. This is a limitation of the core Pheonix* BIOS. The "Network Boot"

selected item in the "Boot" Menu is an unsupported legacy network

boot ROM. The "PXE Support" (BBS) enabling no longer concurrently

updates the "Boot" Menu in this core Pheonix* BIOS.

6. BIOS Boot menu doesn't differentiate between an IDE CD-ROM and USB CDROM boot device.

Problem

BIOS is unable to display the difference between a IDE CD-ROM

and a USB CDROM. Both devices will be displayed as a "CD-ROM

Drive" under <F2> setup "BOOT" sub-menu.

Implication

If you concurrently install an IDE and an USB CD-ROM on SE7500CW2

you will be unable to determine which device is first in the boot-order in

BIOS 1.17 and below.

Workaround

Install the USB and IDE CD-CDROM separately. Between the installation

of first device, say the USB CD-ROM, take note that this is the first device

listed in the boot menu. Reboot and install the IDE CD-ROM. This will

now be the second CD-ROM listed. Devices will be listed according to

the order of installation.

Status Intel is investigating the possibility of fixing this erratum.

7. LDCM 6.3 Wake on LAN not rebooting the server.

Problem Wake on LAN may not reboot the server in the event of a Wake on LAN event.

Implication LDCM may not send or receive Wake on LAN events. This will result in the server

not being powered on as expected.

Workaround Make sure that both NICs are connected to the network. After doing this "Wake

on LAN" will perform as designed.

Status Intel is investigating the possibility of fixing this erratum.

8. Windows 2000* won't install on a Maxtor D540X-4G 137GIG ATA hard-drive

Problem Larger than 137GIG Maxtor ATA hard-drives don't give proper disk space information

in Windows 2000 and are not

recognized during the installation process.

Implication Windows 2000 installation won't find this 137GIG hard-drive. The current Promise drivers won't allow for this hard-

drive to be recognized.

Workaround None

Status Promise RAID driver build 1.14 (PDC20627) allows for this hard-drive to install

Windows 2000. Pending production

release of this driver from Promise, * please

contact Promise* for availability.

9. Adaptec 2100S, 2110S, or 3410S, RAID cards cause LILO to hang during POST with Red Hat 7.3.

Problem	Red Hat Linux 7.3 will fail to boot when an Adaptec 2100S, 2110S, or 3410S,
	RAID card is installed and running Adaptec BIOS 1.60.
Implication	When running the Adaptec* card in "EBDA relocation" mode the system
	will not boot with Adaptec BIOS 1.60. Running Adaptec* BIOS v1.62 in
	conjunction with BIOS 1.17 will provide support for Adaptec* RAID cards
	mentioned above. Once installed it is still necessary to disable
	·
	"EBDA relocation" in the Adaptec* RAID setup.
Workaround	None
Status	Pending production release of BIOS from Adaptec*, please contact Adaptec for availability.

10. LDCM 6.3 build 211 incorrectly lowers processor fan speeds from 6000 RPM to fewer than 2000 RPM.

Problem LDCM 6.3 build 211 incorrectly lowers fan speeds on the SE7500CW2 system only.

Implication Installing and configuring LDCM 6.3 build 211 could possibly create

thermal overheating issues.

Workaround See Technical Adivsory 612-01 for more details and patch availabity.

Status Intel is investigating the possibility of fixing this bug.

11. BIOS 1.17 incorrectly sets the BIOS EDBA memory area to 0 bytes.

Problem Without EBDA BIOS memory allocation, PCI-based cards that require this space

may have inconsistent performance.

Implication Certain cards like High-Availibility adapters may fail.

Workaround None

Status Fixed in BIOS 1.23.

12. BIOS 1.17, 1.18 NIC disabling switch turns off the wrong NIC.

Problem If you disable NIC1 in F2 BIOS then NIC2 is turned off. If you disable NIC2 in F2

BIOS NIC1 is turned off. You will see this with the NIC LEDs on rear and

on the SC5200 front panel NIC lights.

Implication The wrong NIC could be disabled accidentally

Workaround None

Status Fixed in BIOS 1.23.

13. UUID not programmed on TA A88031-505, A88029-004, and A88030-003 below boards (PBA A87967-506).

Problem SyMBIOS UUID (unique board identifier) has not been programmed at the factory. This may

make it difficult for such programs like Linux High Performance Clusters (HPC) to work properly.

Implication The only way to uniquely identify a SE7500CW2 system board is by reading the bar

code number sticker next to the Onboard Promis RAID chip (PDC20267). An

example of the unique identifier would be BPCW23701091.

Workaround None.

Status To be correctly programmed on A88031-507, A88029-007, and A88030-006 boards

in early Q1 '2003. See PCN #103036-01 (ECO #6052488) for more details.

14. Logical processors are no longer listed in BIOS POST if hyper-threading is enabled in F2 BIOS setup.

ыоз	setup.
Problem	Logical processors are not listed in BIOS 1.18 and above even if
	hyper-threading is enabled in BIOS. Logical processrs are no longer
	mentioned with the text string of "4 Logical Intel® Xeon™ 2.8 Ghz processors"
	if hyper-threading is enabled with two processors populated.
Implication	There may be confusion as to whether hyper-threading it really working.
Workaround	None
Status	The change has been implemented in BIOS 1.23 and above. This is by design
	and now the text string reads "Intel® Xeon™ Processors MP 2.8GHz" even if hyperthreading
	is enabled. The number of logical processors is no longer listed. Only the printed POST
	string has changed, but the functionality of hyper-thread remains identical in BIOS.

Documentation Errata

1. Shock and Vibe test results aren't are mentioned in the Technical Product Specification

Problem Shock and Vibe test results aren't mentioned in the most recent Technical Product

Specification published in September, 2002.

Implication Without this information it may be difficult to explain the rigorous testing that

SE7500CW2 server board in the SC5200 450W base chassis has endured.

Workaround The test results are listed below:

Shock and vibe testing is a rigorous set of tests which tests board strength

and durability under extreme conditions. We have tested the SC5200 Base

450W chassis with SE7500CW2 board and the results are as follows:

- Shock operatin test passed
- Shock non-operating test failed. Intel is currently investigating this issue further.
- Vibration operating test passed.
- Vibration non-operating test passed.

Status This will be corrected in the next quarterly update of the SE7500CW2

Technical Product Specification.

2. Intel® 53C1000B1 SCSI card's LED pin-out is not mentioned in the Technical Product Specification (TPS).

Problem

No pin-out for the J1 4-pin header as bundled with the SE7500SCSI SKU SCSI

card is mentioned in the TPS.

Implication Without

Without the pin-out it is impossible to create a cable to enable hard-drive LEDs.

Workaround

The pin-out of the device is as follows:

Pin1 - +5V

Pin2 – LED1_L

Pin3 – LED1 L

Pin4 -- +5V

Status

To be updated in a future version of the TPS.

3. The TPS doesn't contain information explaining why if an additional Video adapter as added to the system the onboard video is disabled.

Problem

Board users will attempt to disable onboard video controllers in BIOS eventhough a

switch doesn't exist. Though no switch exists in BIOS the onboard device will

automitically be disabled if an add-in video card is added.

Implication Confusion on the functionality of the onboard video when an add-in video card is

added.

Workaround None

Status To be fixed in a future version of the TPS.

4. The TPS doesn't explain with BIOS Beep Code 4-3-1-4.

Problem The action require to fix BIOS Beep code 4-3-1-4 is undetermined since it is not

mentioned in the TPS. Beep code 4-3-1-4 indicates that no memory DIMM pair is

present.

Implication Confusion over the beep code 4-3-1-4. To prevent the beep code it is necessary to

place DIMMs in pairs; either DIMM pair 1A/1B or DIMM pair 2A/2B.

Workaround None

Status To be fixed in a future version of the TPS.