



Intel® Server Board SHG2

Specification Update

Intel Order Number: C20107-002

January 2003



Enterprise Platforms and Services Marketing

Revision History

Date	Modifications
9/11/02	Initial release.
10/16/02	Added errata 13-15. Updated errata 1, 2, 3, 6, 8, and 9. Added documentation change 4.
11/13/02	Moved errata 4, 8, 9, 10, and 14 to the SHG2 Tested Hardware & OS List document Rev. 3.0. Added erratum 11.
12/11/02	Moved errata 1, 2, 3, 4, 5, 9, and 10 to the SHG2 Technical Product Specification (TPS) Rev. 2.0. Incorporated all documentation changes into the SHG2 TPS Rev. 2.0.
1/15/03	Changed the status of errata 1 and 3 from Fix to NoFix.

Disclaimers

The Intel® Server Board SHG2 may contain design defects or errors known as errata that may cause the product to deviate from the published specifications. Current characterized errata are documented in this Specification Update.

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Preface

This document is an update to the specifications contained in the *SHG2 Technical Product Specification* (Order Number C11343-001). It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools. It will contain specification changes, specification clarifications, errata, and document changes.

Refer to the *Intel® Xeon™ Processor Specification Update* (Order Number 249678-018) for specification updates concerning the Intel® Xeon™ processor. Items contained in the *Intel® Xeon™ Processor Specification Update* that either do not apply to the Intel® Server Board SHG2 or have been worked around are noted in this document. Otherwise, it should be assumed that any processor errata for a given stepping are applicable to the Printed Board Assembly (PBA) revisions(s) associated with that stepping.

Nomenclature

- **Specification Changes** are modifications to the current published specifications for the SHG2 server boards. These changes will be incorporated in the next release of the specifications.
- **Specification Clarifications** describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.
- **Documentation Changes** include typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.
- **Errata** are design defects or errors. Errata may cause the SHG2 server board's behavior to deviate from published specifications. Hardware and software designed to be used with any given processor stepping must assume that all errata documented for that processor stepping are present on all devices.

Product Scope

Below are the specific boards, BIOS and components covered by this update.

Baseboard FAB #	Baseboard PBA #	BIOS	Baseboard Management Controller (BMC) Firmware	Processor Stepping	Chipset Stepping (ServerWorks* GCLE ServerSet*: CMIC-LE, CIOB-X2, & CSB5)
FAB 5	A77226-504	Production Release v. 1.03, Build 29	BMC v. 14	B0, C1	CMIC-LE: A2.0 CIOB-X2: A1.3 CSB5: A2.1
FAB 5	A77226-505	Production Release v. 1.03, Build 29	BMC v. 14	B0, C1	CMIC-LE: A2.0 CIOB-X2: A1.3 CSB5: A2.1
FAB 5	A77226-506	Production Release v. 1.03, Build 29	BMC v. 14	B0, C1	CMIC-LE: A2.0 CIOB-X2: A1.3 CSB5: A2.1
FAB 5	A77226-507	Production Release v. 1.05, Build 31	BMC v. 20	B0, C1	CMIC-LE: A2.0 CIOB-X2: A1.3 CSB5: A2.1

Summary Tables of Changes

The following tables indicate the errata and the document changes that apply to the Intel® Server Board SHG2. Intel intends to fix some of the errata in a future stepping of components, and to account for the other outstanding issues through documentation or specification changes as noted. The tables use the following notations:

Doc: Intel intends to update the appropriate documentation in a future revision.

Fix: Intel intends to fix this erratum in a future release of the component.

Fixed: This erratum has been previously fixed.

NoFix: There are no plans to fix this erratum.

Shaded: This erratum is either new or has been modified from the previous specification update.

Table 1. Errata Summary

No.	Plans	Description of Errata
1.	NoFix	Microsoft Windows* 2000 system information utility reports incorrect information following a BIOS, BMC firmware, and FRU/SDR file update
2.	Fix	Connecting or disconnecting a USB device does not cause the SHG2 system to come out of S1 sleep state
3.	NoFix	Failure to expand Option ROM
4.	Fix	BMC error when running SHG2 platform confidence test (PCT) v. 1.00

Table 2. Documentation Changes

No.	Plans	Description of Documentation Change
1.		

Following are in-depth descriptions of each erratum / documentation change indicated in the tables above. The errata and documentation change numbers below correspond to the numbers in the tables.

Errata

1. Microsoft Windows* 2000 system information utility reports incorrect information following a BIOS, BMC firmware, and FRU/SDR file update

Problem: After updating the BIOS, BMC firmware, and FRU/SDR files on the SHG2 server board, the Microsoft Windows 2000 system information utility displays incorrect values for “System Model” and “BIOS Version” items.

Implication: The Microsoft Windows 2000 system information utility does not display the correct values for “System Model” and “BIOS Version” items following a BIOS, firmware, and FRU/SDR file update.

Workaround: None.

Status: NoFix.

2. Connecting or disconnecting a USB device does not cause the SHG2 system to come out of S1 sleep state

Problem: A USB wake on connect should occur if at least one USB device is connected to the SHG2 server system on one of the ports and then a second USB device is either connected or disconnected from the system in the S1 sleep state. However, with one USB device connected, either connecting or disconnecting a second USB device from the SHG2 in the S1 sleep state does not cause the system to come out of the S1 sleep state.

Implication: The ServerWorks* CSB5 chipset driver does not configure the USB controller properly for wake events on the USB ports.

Workaround: None.

Status: Fix. Intel is currently working with ServerWorks to investigate a fix for this issue.

3. Failure to expand Option ROM

Problem: When configuring an SHG2 based system with adapters containing option ROMs an error message may be displayed during the boot process similar to the following:

```
ERROR
```

```
Expansion ROM not initialized - PCI Mass Storage  
Controller in slot 3
```

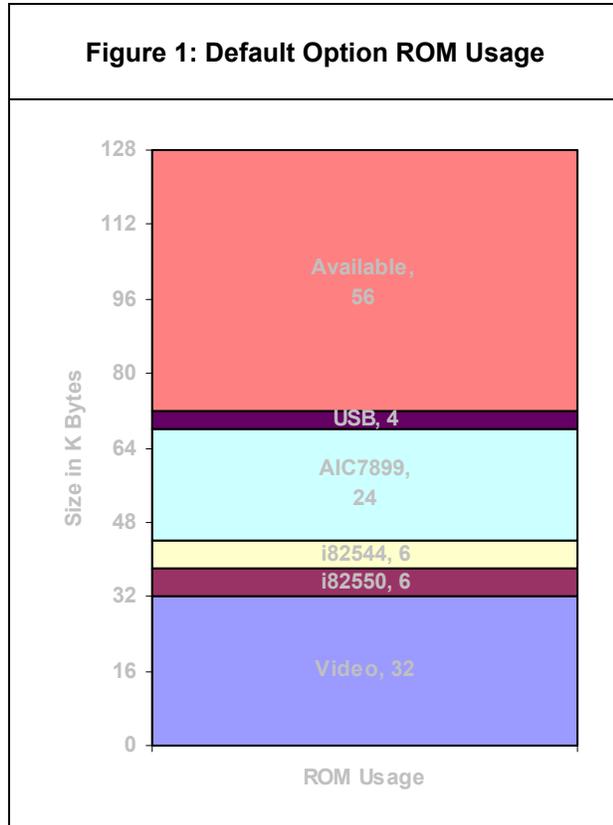
This issue can be observed with as few as one adapter card installed in the system.

Implication: The amount of space reserved by the system for Option ROMs is limited to 128K on SHG2 based systems. This space is shared by the on-board device option ROMs and any add-in adapter option ROMs. The on-board devices are: video, gigabit NIC, 10/100 NIC, SCSI controller, and USB. All of the on-board option ROMs are enabled by default with the exception of USB.

When all of the on-board option ROMs are loaded at boot time, there is a reduced amount of reserved space left for add-in adapter card option ROMs to expand and load (see *Figure 1*). If enough space does not exist for a particular adapter, that adapter's option ROM will fail to expand and will post an error message during system boot.

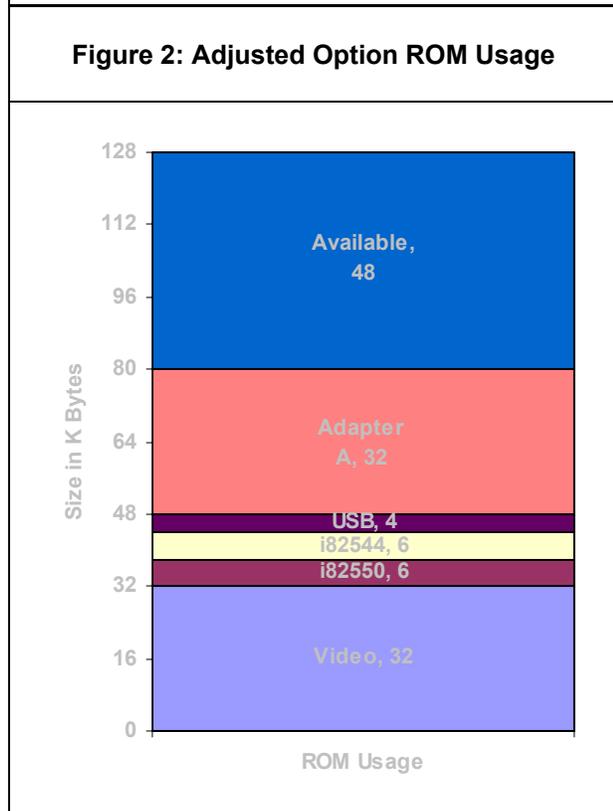
It is important to note that option ROM expansion typically requires two different amounts of memory. There is an initial memory request for memory and there is a final memory consumed. The initial memory request is almost always more than the final amount of memory required.

For example, assume *Adapter A's* (a SCSI adapter) option ROM requests 64K of initial memory and then reduces the final amount of memory used to 32K. In the example in *Figure 1*, the *Adapter A's* option ROM expansion would fail because the initial request for memory was 64K while 56K is available.



In order to enable Adapter A's option ROM to load, adjustments need to be made to the option ROM usage area. Since Adapter A is a SCSI adapter, in this example it is determined that the on-board 7899 SCSI controller option ROM can be disabled because it is not going to be utilized as a boot device. By disabling the on-board 7899 option ROM, 24KB of space is release giving a total of 80KB. In this configuration Adapter A will pass the initial request of 64KB space, reduce to 32KB, and will successfully load leaving a memory usage map similar to that shown in Figure 2.

Option ROMs, although enabled by default, are not required in many situations. Typically, the only time option ROMs are required is if the option ROM is supporting a boot device or the option ROM is supporting a RAID configuration. Most other configurations do not require the option ROM to be enabled to provide device functionality.



SCSI devices (such as the on-board 7899) do not need to have the option ROM enabled in order to function. The only time SCSI devices require the option ROM is when it is required to boot from drives attached to the SCSI controller. Likewise, NIC controllers such as the i82544 do not require the option ROM for functionality such as *adapter teaming*; the option ROM is only required to support PXE booting from the network.

Workaround: Intel recommends that option ROM scanning be disabled for any device or PCI slot that does not require the option ROM for a boot device, or other functionality such as RAID management.

The option ROMs for each on-board device and for each PCI slot can be enabled or disabled through BIOS Setup. Option ROM scanning is enabled by default for all on-board devices and for all PCI slots. To enter BIOS Setup press F2 during system boot.

To disable option ROM scanning for any device, enter BIOS Setup and go to the Advanced > PCI Configuration menu. This menu will display selections for the four embedded devices (SCSI, NIC 1, NIC 2, Video) and each of the eight PCI slots. Select the device for which the option ROM scan should be disabled and select "disable" from the "Option ROM Scan" field.

Status: NoFix.

4. BMC error when running SHG2 platform confidence test (PCT) v. 1.00

Problem: The following error may appear when running SHG2 PCT v. 1.00 on a SHG2 server system with a single processor configuration. The issue does not appear on a dual processor configuration:

```
*** ERROR BMC.PROCESSORCFG 4.15.1.0116
BMC command 'Get Sensor Reading' Failed
Processor 2 Stat Sensor 99h
Completion Code CBh – BMC Sensor does not exist
Standard Error Code = 0EE03035
(Error logged at 10-10-02 13:14:14)
BMC.PROCESSORCFG FAILED
```

Implication: This issue is a test software issue, and does not affect the functionality of the SHG2 server board.

Workaround: None.

Status: Fix. Intel is currently investigating a BMC firmware and PCT software fix for this issue.

Documentation Changes

None at this time.